

**Figure 1**  
(Prior Art)

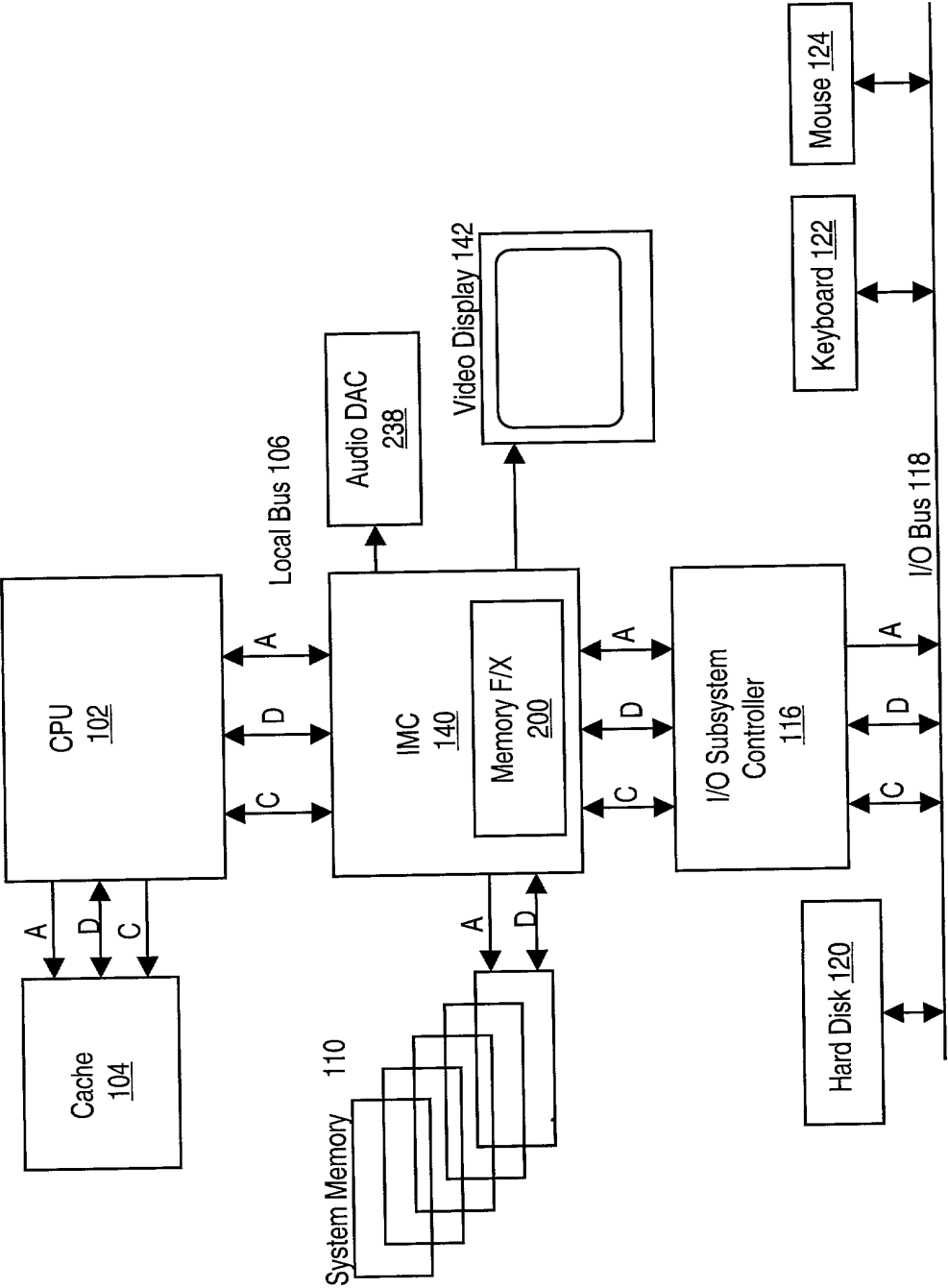


Figure 2A

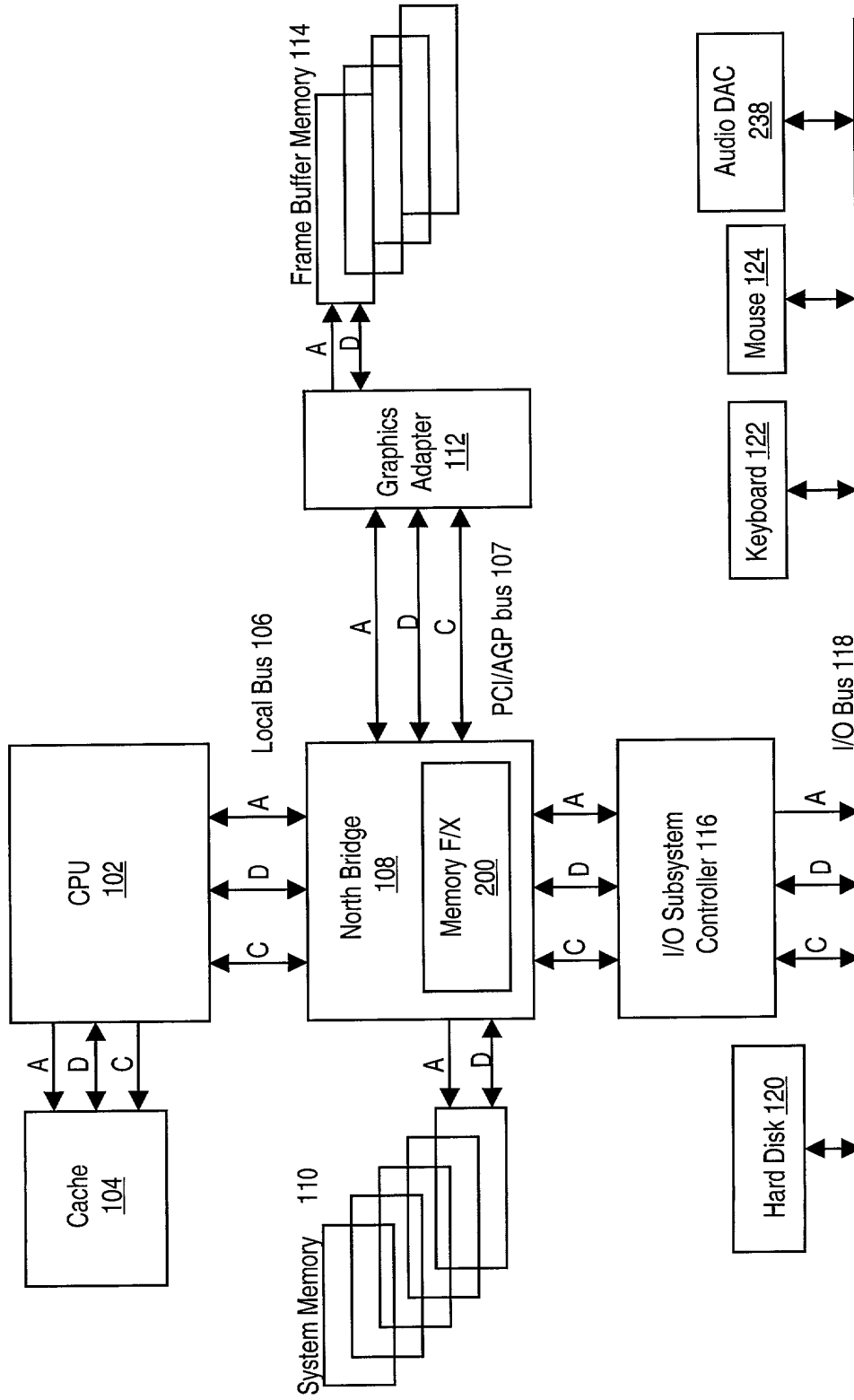


Figure 2B

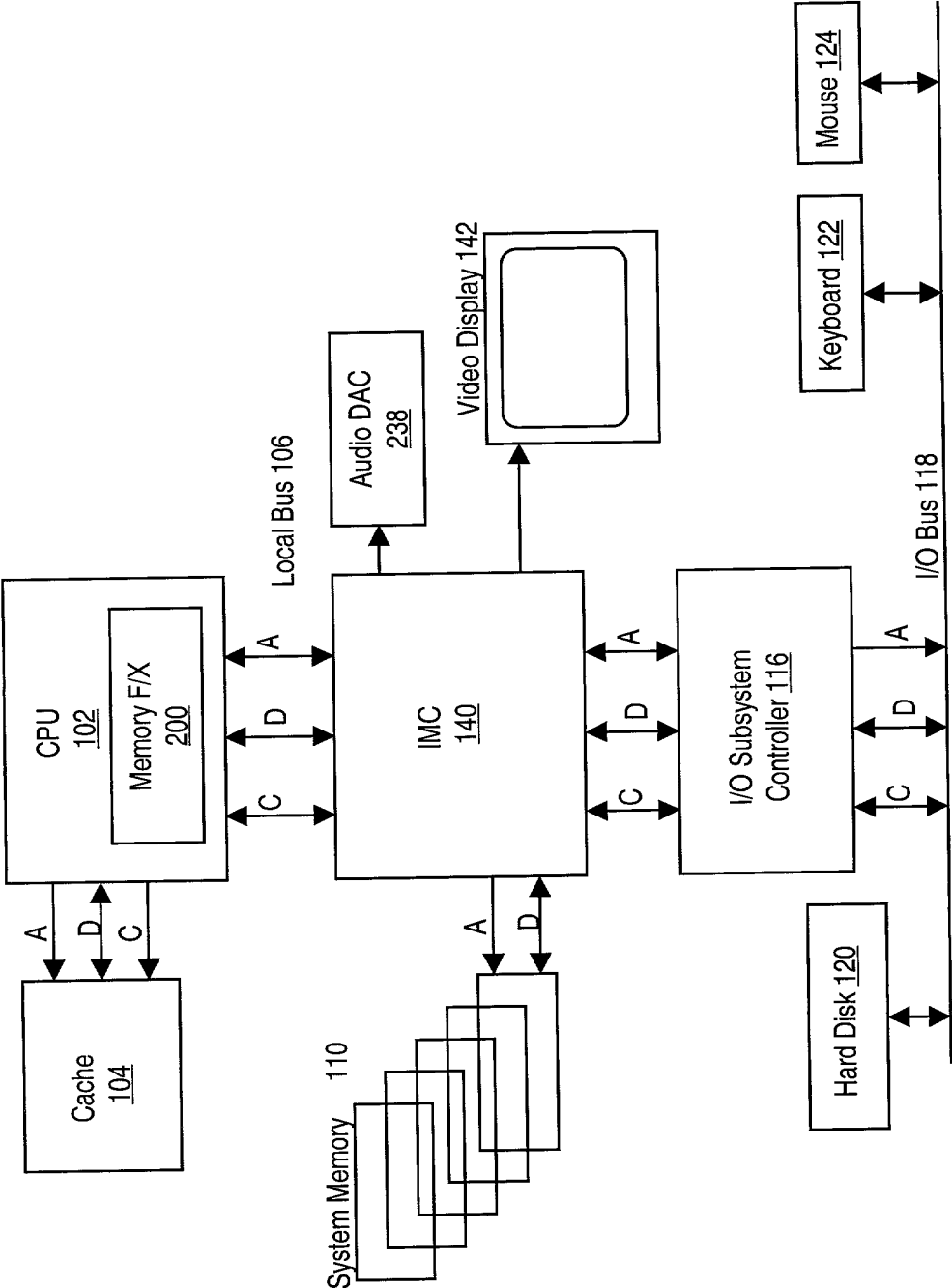


Figure 2C

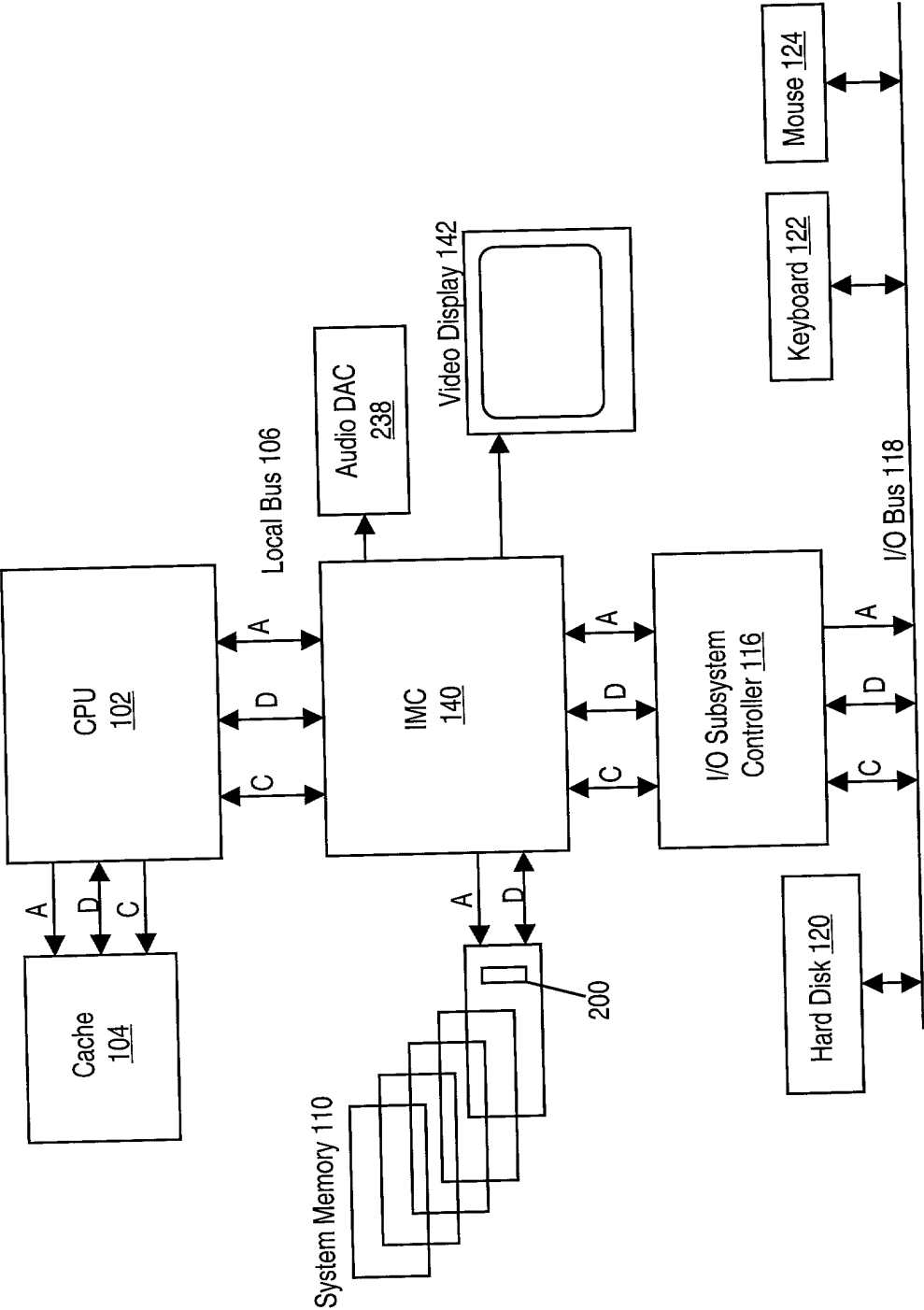


Figure 2D

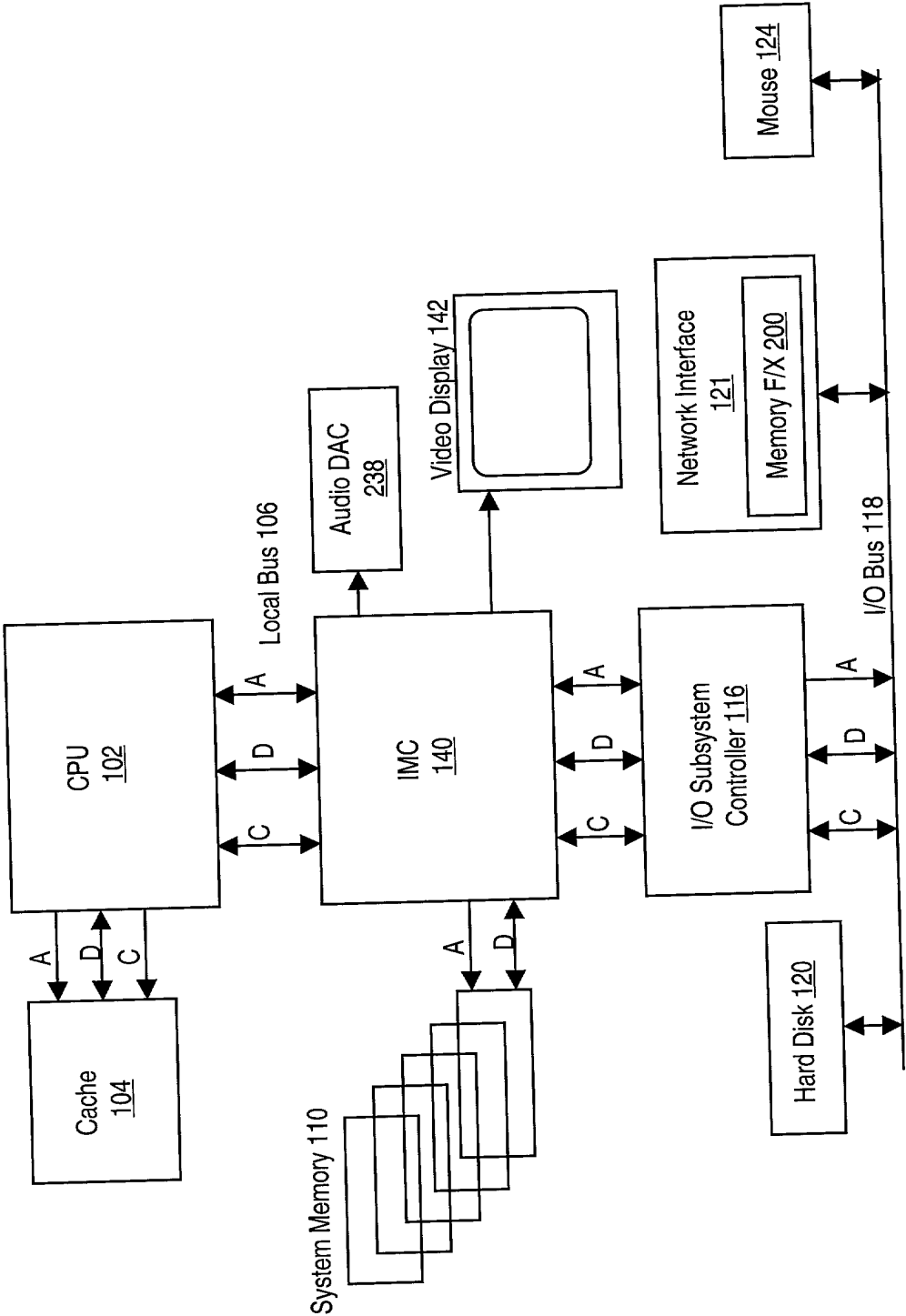
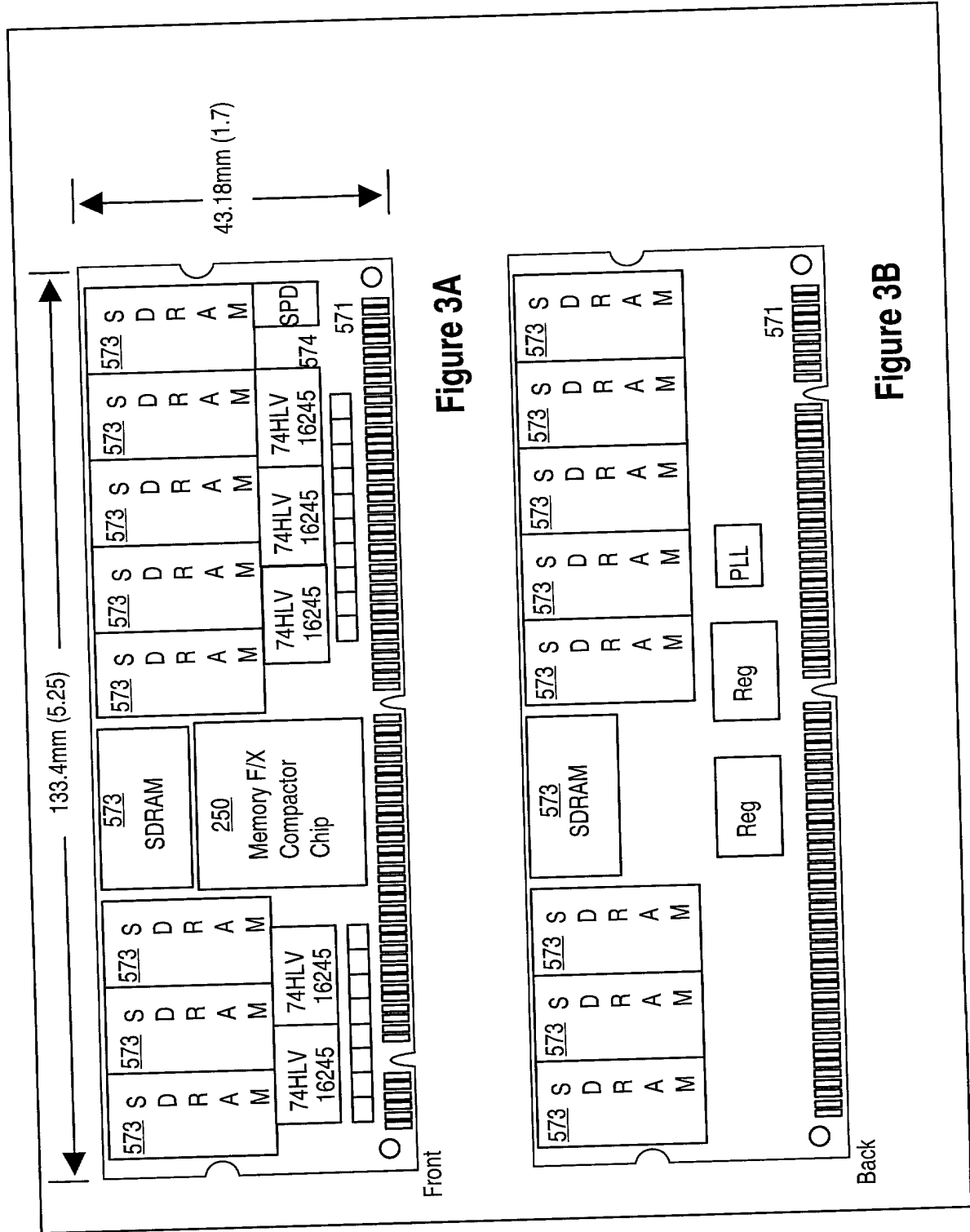
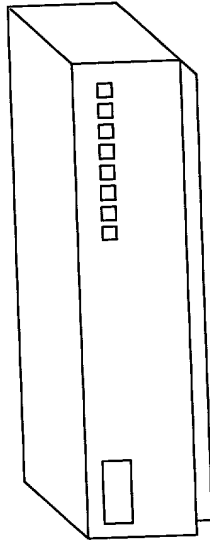


Figure 2E

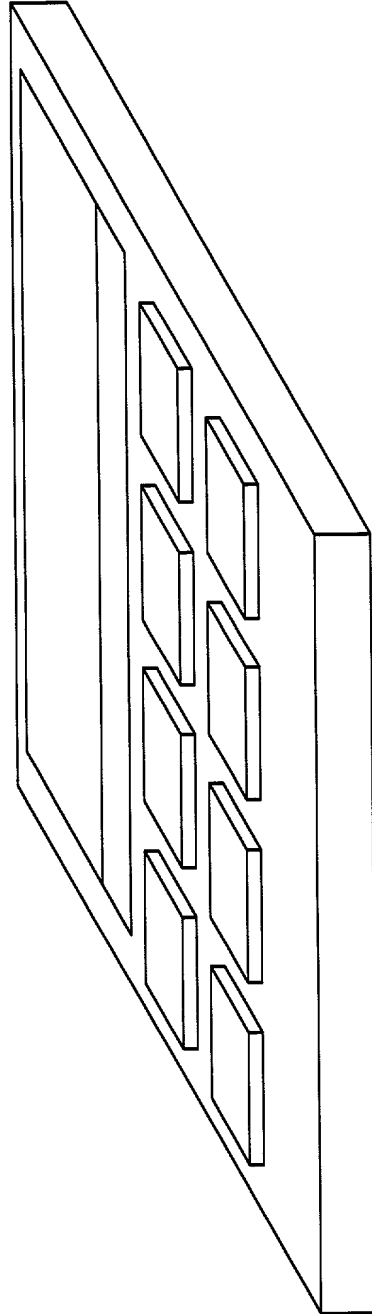




Router 130

Figure 4





PDA

**Figure 5**

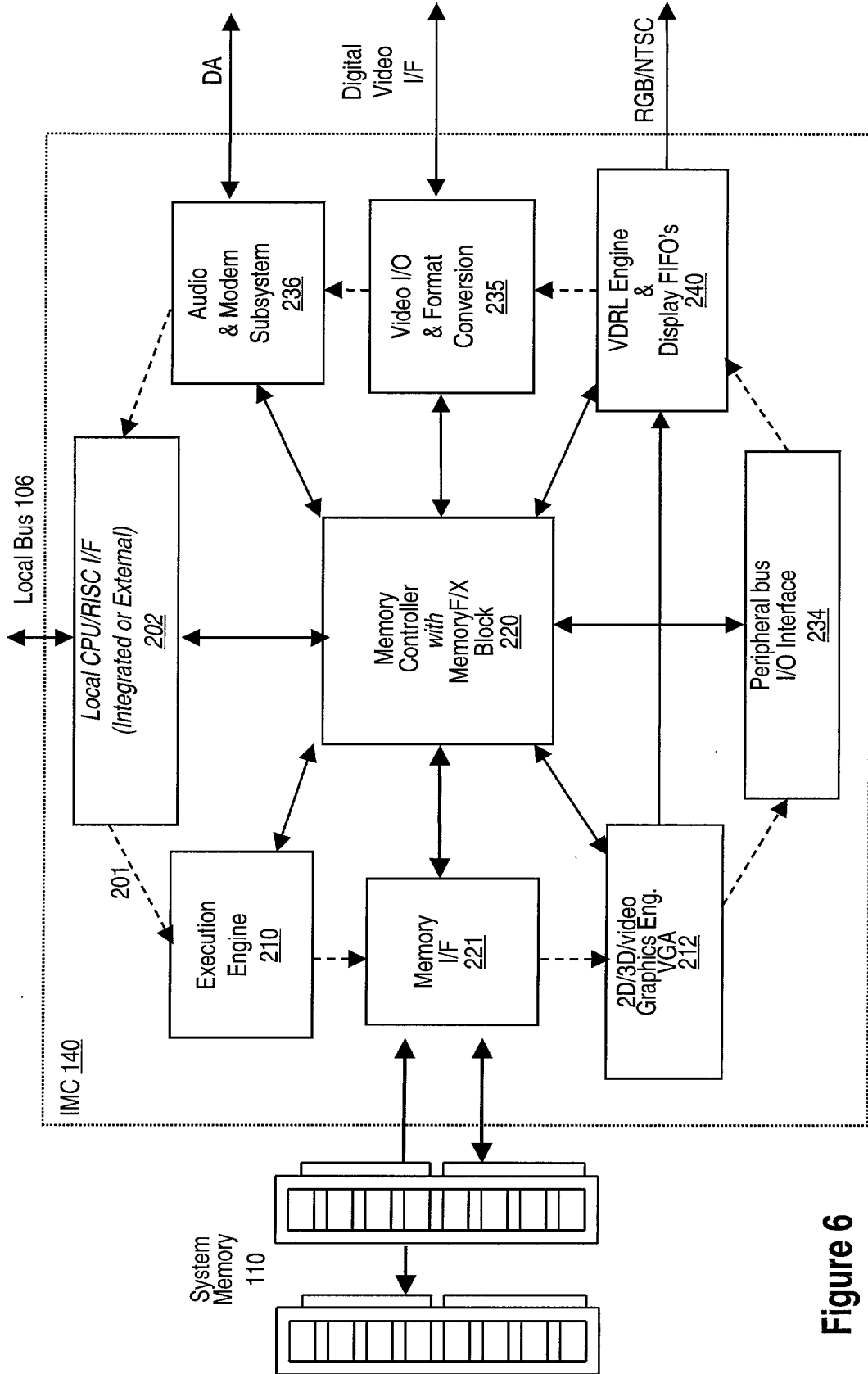


Figure 6

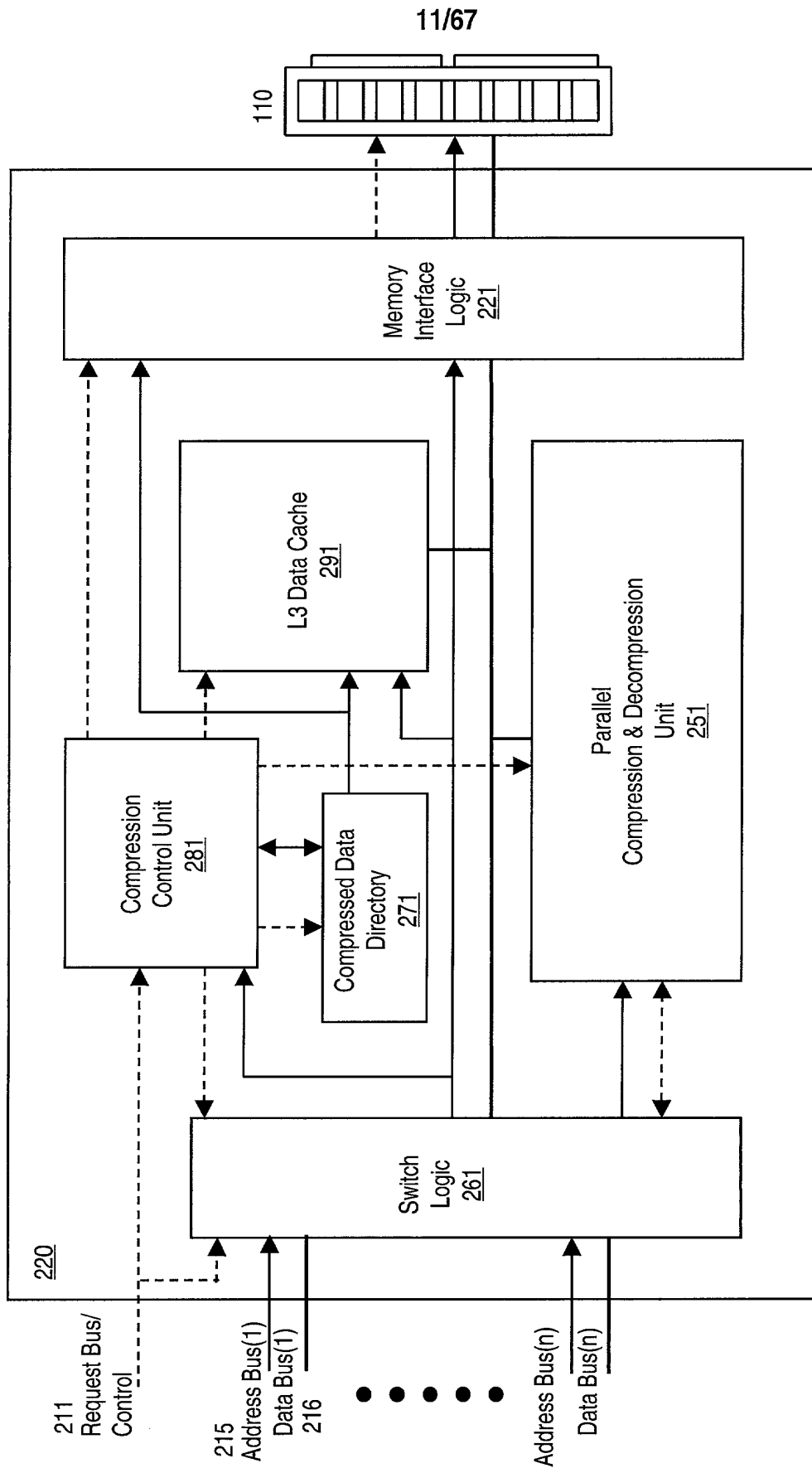


Figure 7

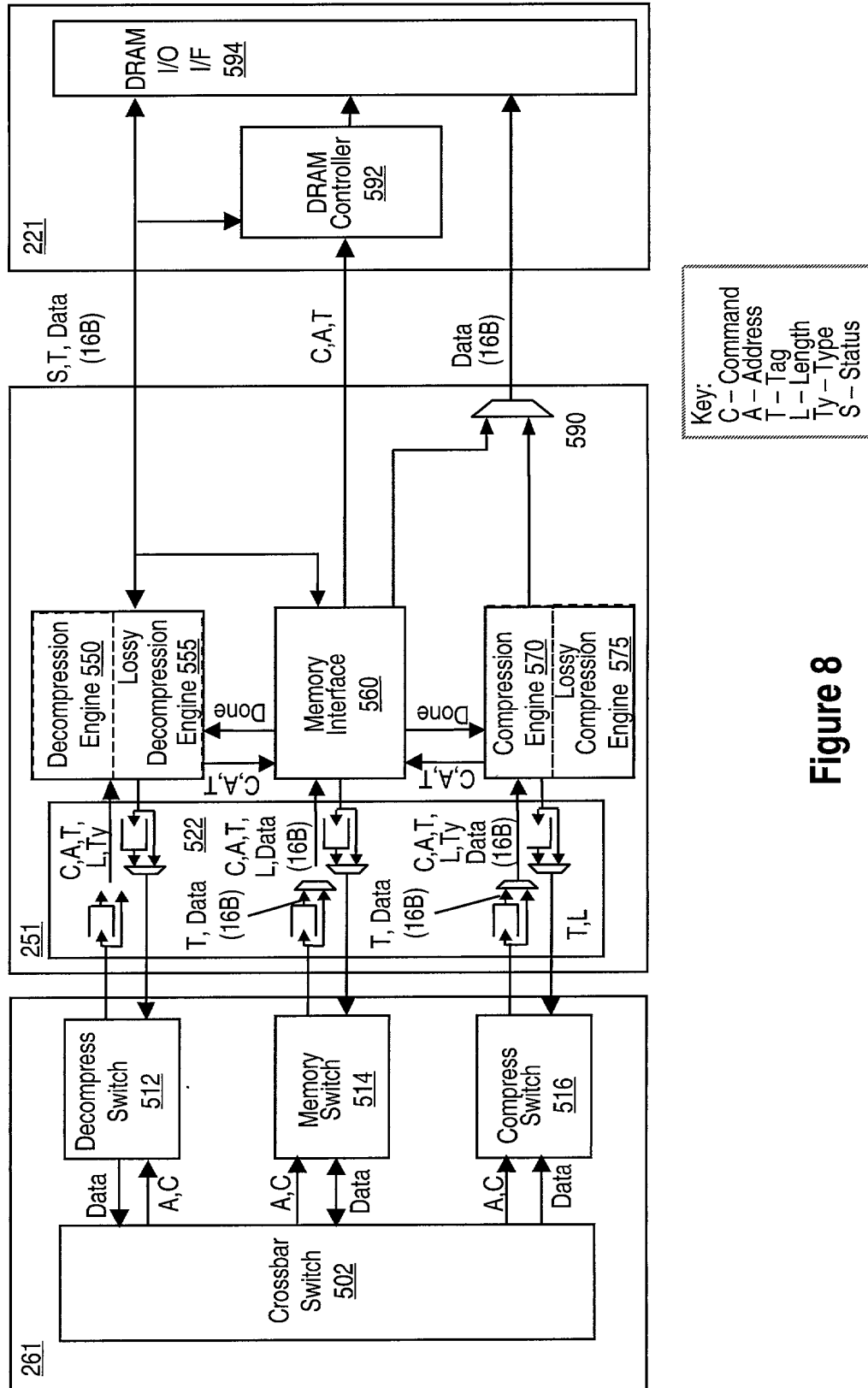
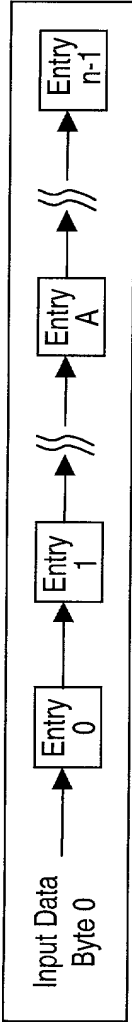
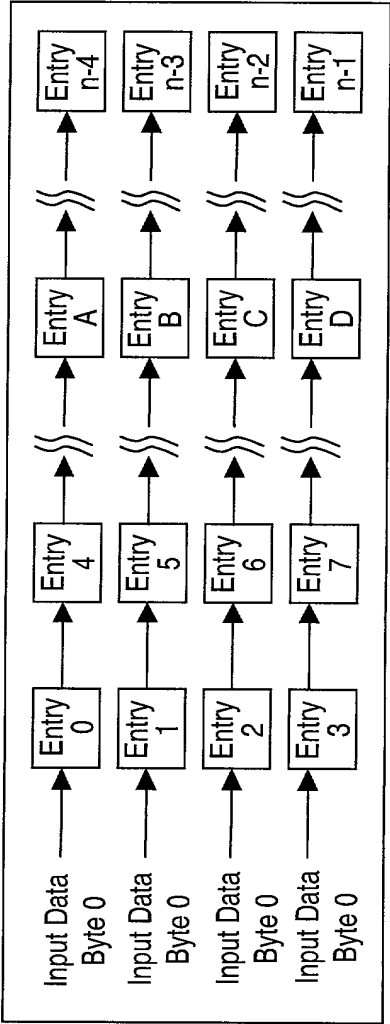


Figure 8



**Figure 9A**  
( Prior Art)



**Figure 9B**  
( New Art)

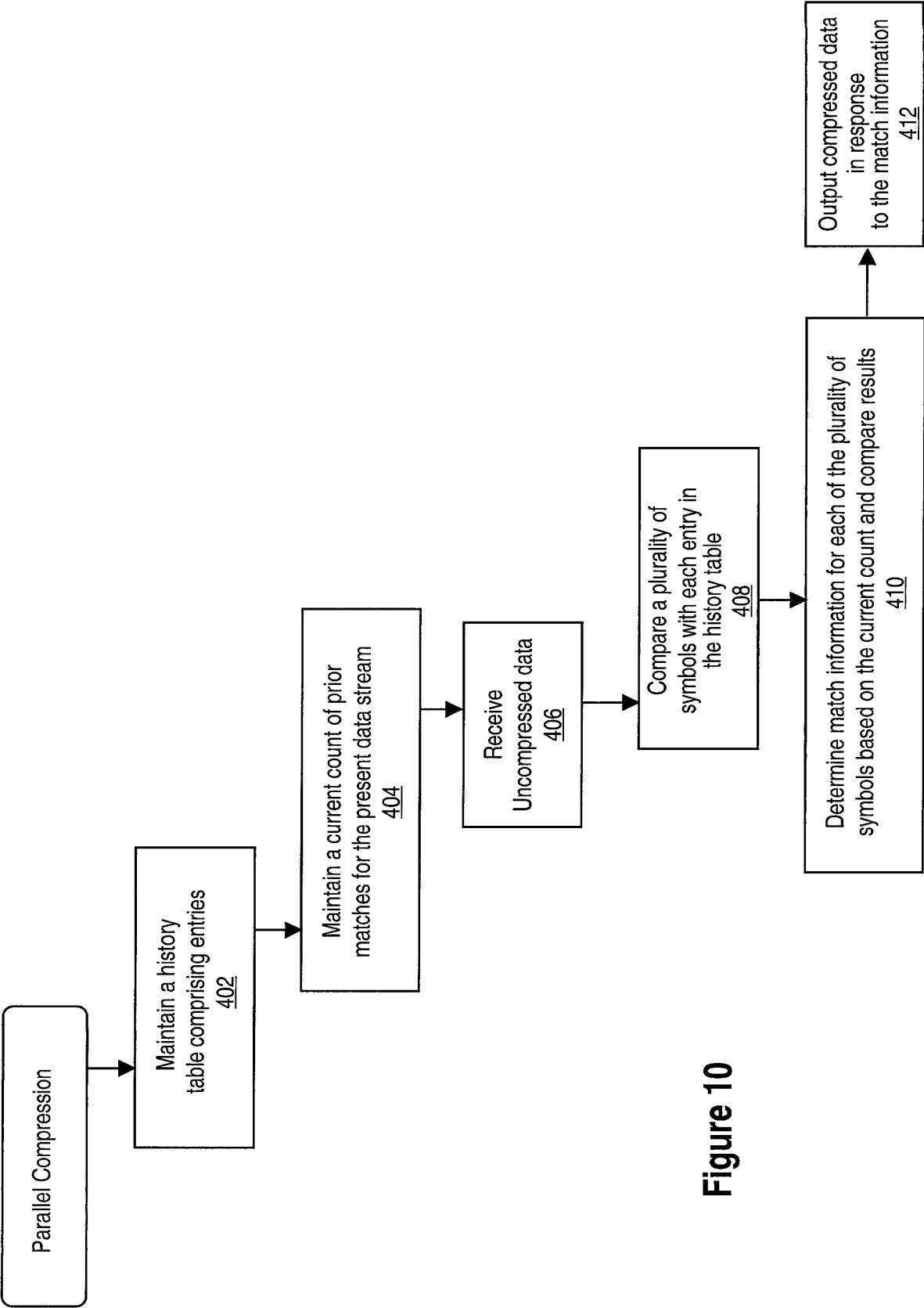
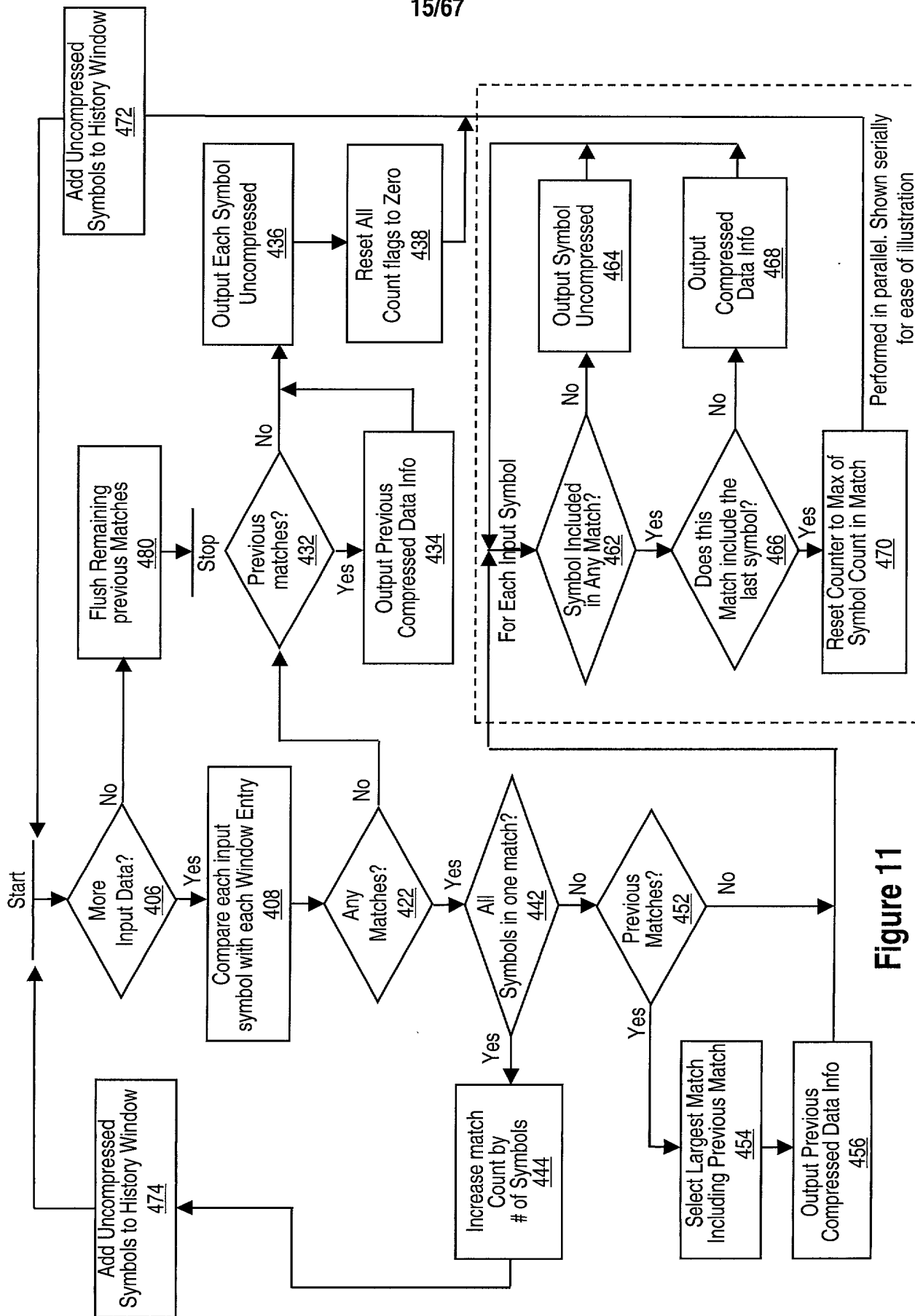


Figure 10



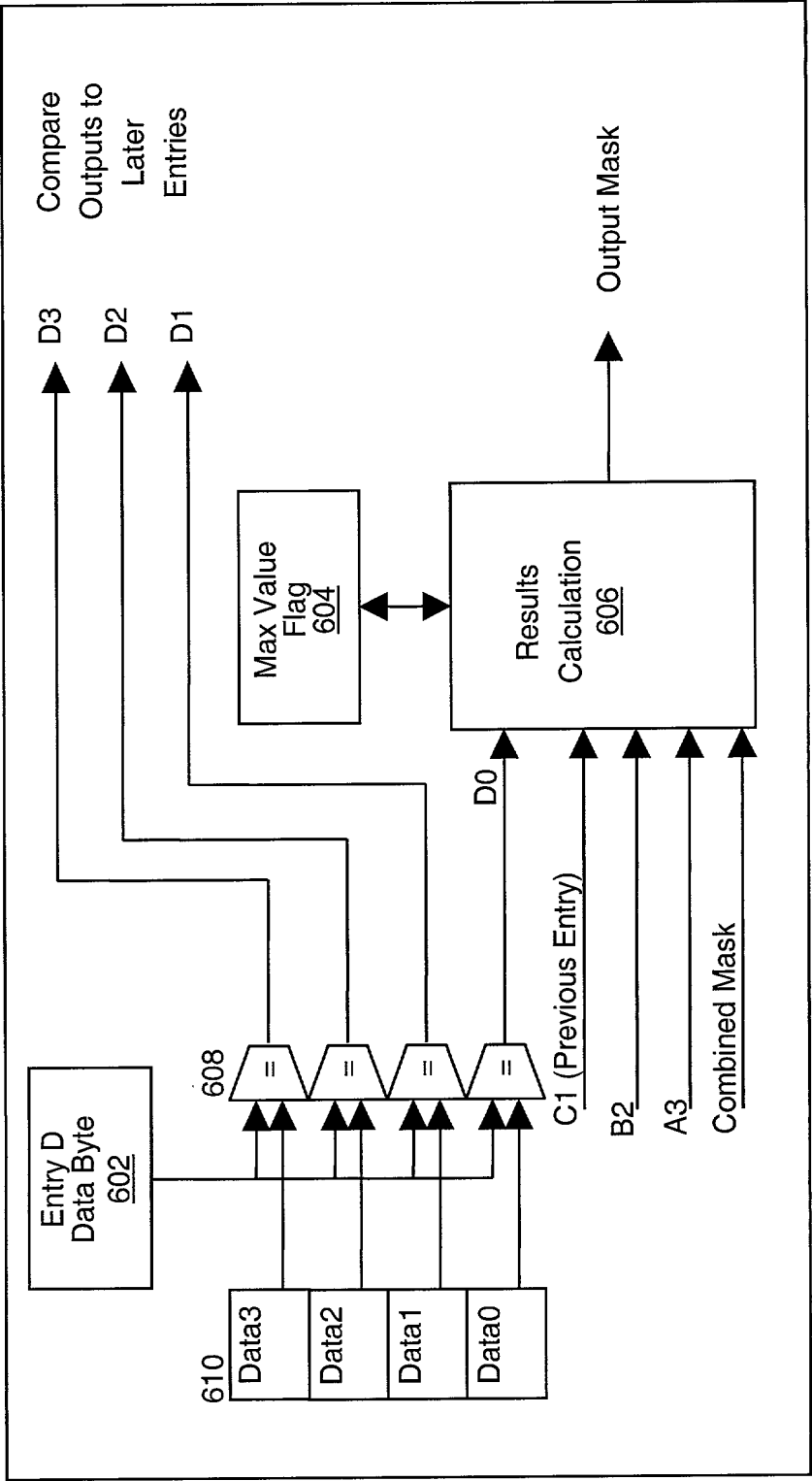


Figure 12



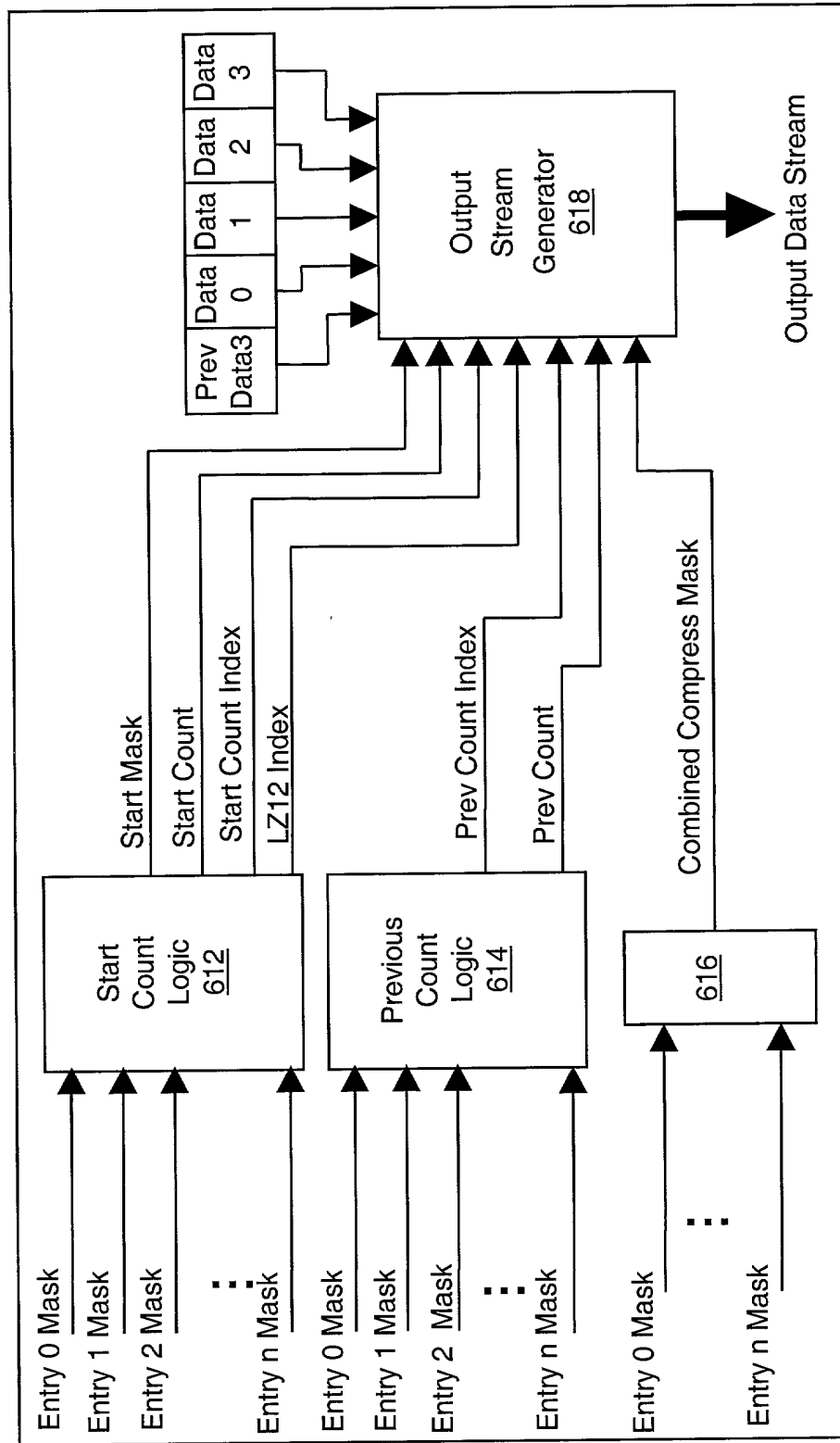


Figure 13

Input Matches				Output
D0	C1	B2	A3	
1	1	1	1	Mask
1	1	1	0	1111
1	1	0	1	1110
1	1	0	0	1101
1	0	1	1	1100
1	0	1	0	1011
1	0	0	1	1010
1	0	0	0	1001
0	1	1	1	1000
0	1	1	0	0111
0	1	0	1	0110
0	1	0	0	0101
0	0	1	1	0100
0	0	1	0	0011
0	0	0	1	0010
0	0	0	0	0001
0	0	0	0	0000

Figure 14a

Combined Mask	Count
0000	0
0001	1
0010	0
0011	2
0100	0
0101	1
0110	0
0111	3
1000	0
1001	1
1010	0
1011	2
1100	0
1101	1
1110	0
1111	Count+4

Figure 14b

Output Masks	Combined Mask
M1234   4321 & ~M1	0001
432 & ~M12	0010
43 & ~M123	0100
4 & ~M1234	1000
First valid row determines Combined Mask Output	
M-Max Count Flag 1-1 <sup>st</sup> Symbol Match 2-2 <sup>nd</sup> Symbol Match 3-3 <sup>rd</sup> Symbol Match 4-4 <sup>th</sup> Symbol Match	

Figure 14c

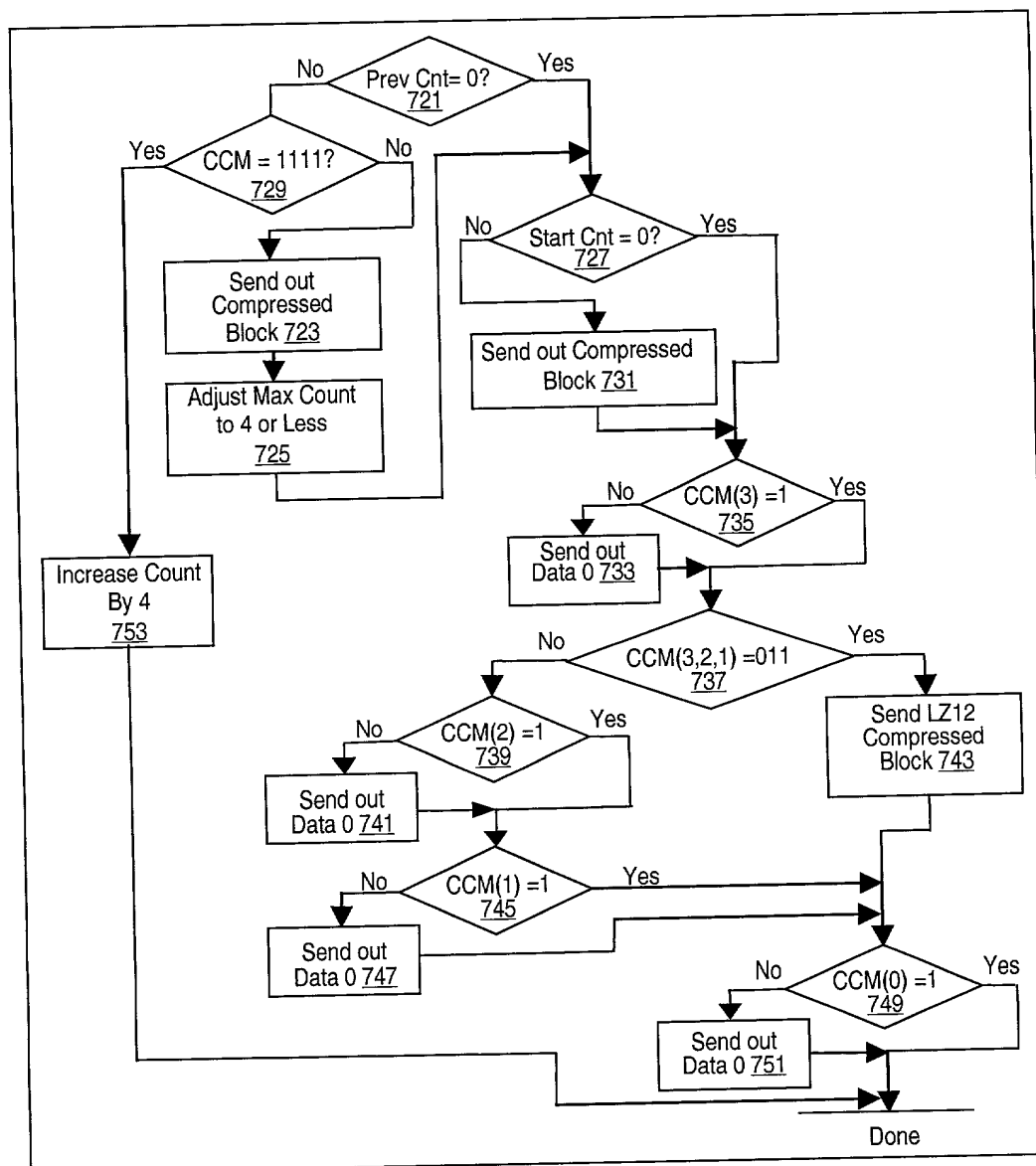


Figure 15

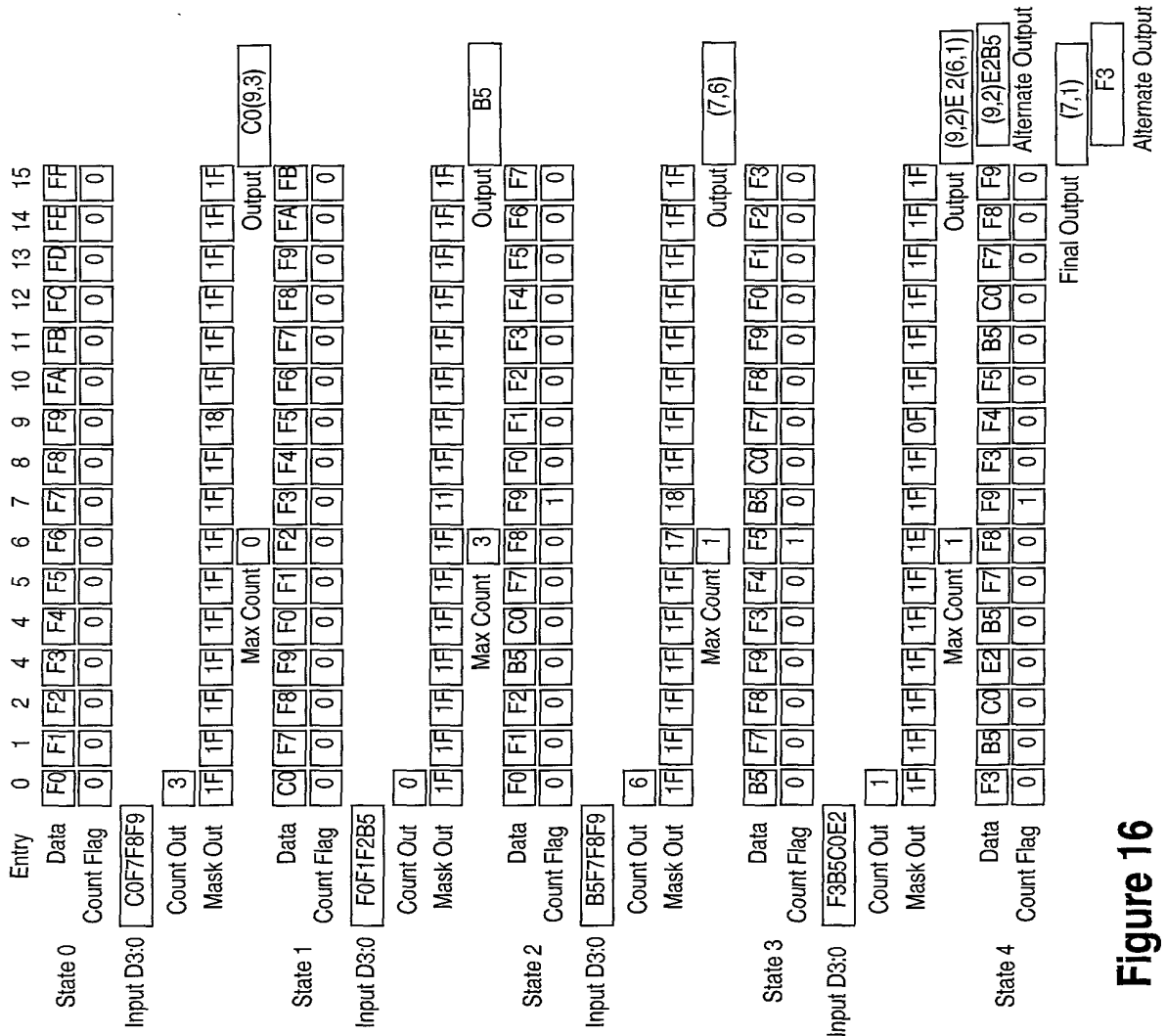


Figure 16

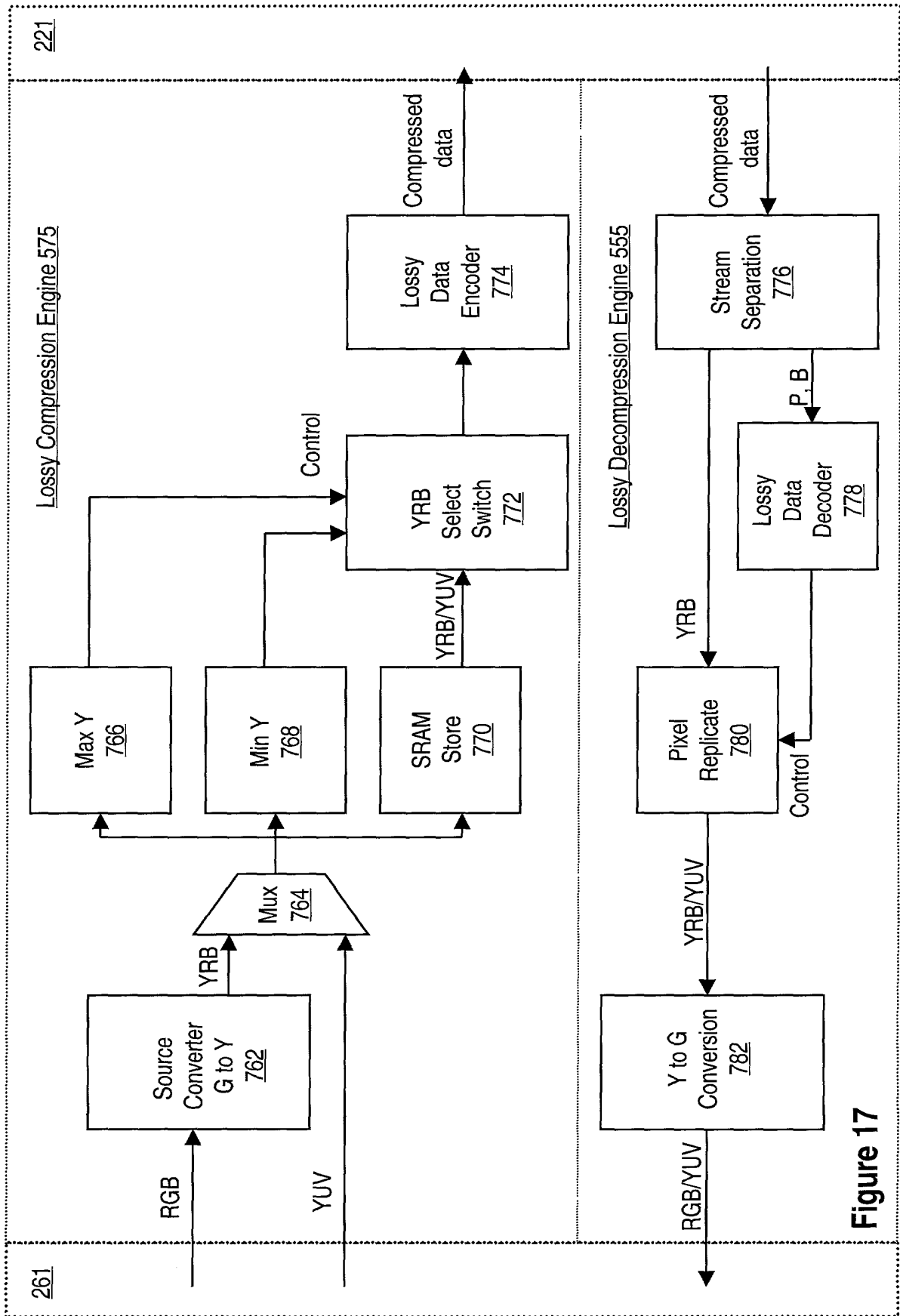


Figure 17

Ymax = Ymin	1 color	Ymax 6 bits	Ymax 6 bits	Rmax 5 bits	Bmax 5 bits	11 2 bits	3 Bytes
Ymax != Ymin	2 colors	Ymax 6 bits	Ymin	Rmax 5 bits	Rmin 5 bits	Bmax 5 bits	P bits 16 bits
Ymax != Ymin	>2 colors	Ymin 6 bits	Ymax 6 bits	Rmax 5 bits	Rmin 5 bits	Bmax 5 bits	P bits 32 bits

Figure 18

Ymax = Ymin	Amax = Amin = 0x00	1 color	Ymax 6 bits	Ymax 6 bits	Rmax 5 bits	Bmax 5 bits	00 2 bits			3 Bytes
Ymax = Ymin	Amax = Amin = 0xFF	1 color	Ymax 6 bits	Ymin	Rmax 5 bits	Bmax 5 bits	11 2 bits			3 Bytes
Ymax = Ymin	Amax = Amin != 00 or FF	1 color	Ymax 6 bits	Ymax 6 bits	Rmax 5 bits	Bmax 5 bits	01 2 bits	Amin 4/8 bits		4/5 Bytes
Ymax = Ymin	Amax != Amin	1 color	Ymax 6 bits	Ymin	Rmax 5 bits	Bmax 5 bits	01 2 bits	Amin 4/8 bits	P bits	6/7 Bytes
Ymax = Ymin	Amax != Amin	2 Alphas	Ymax 6 bits	Ymin	Rmax 5 bits	Bmax 5 bits	10 2 bits	Amin 4/8 bits	P bits	8/9 Bytes
Ymax != Ymin	X	2 colors	Ymax 6 bits	Ymin	Rmax 5 bits	Bmax 5 bits	01 2 bits	Amin 4/8 bits	P bits	7/8 Bytes
Ymax != Ymin	X	>2 colors	Ymax 6 bits	Ymin	Rmax 5 bits	Bmax 5 bits	01 2 bits	Amin 4/8 bits	P bits	9/10 Bytes

Figure 19

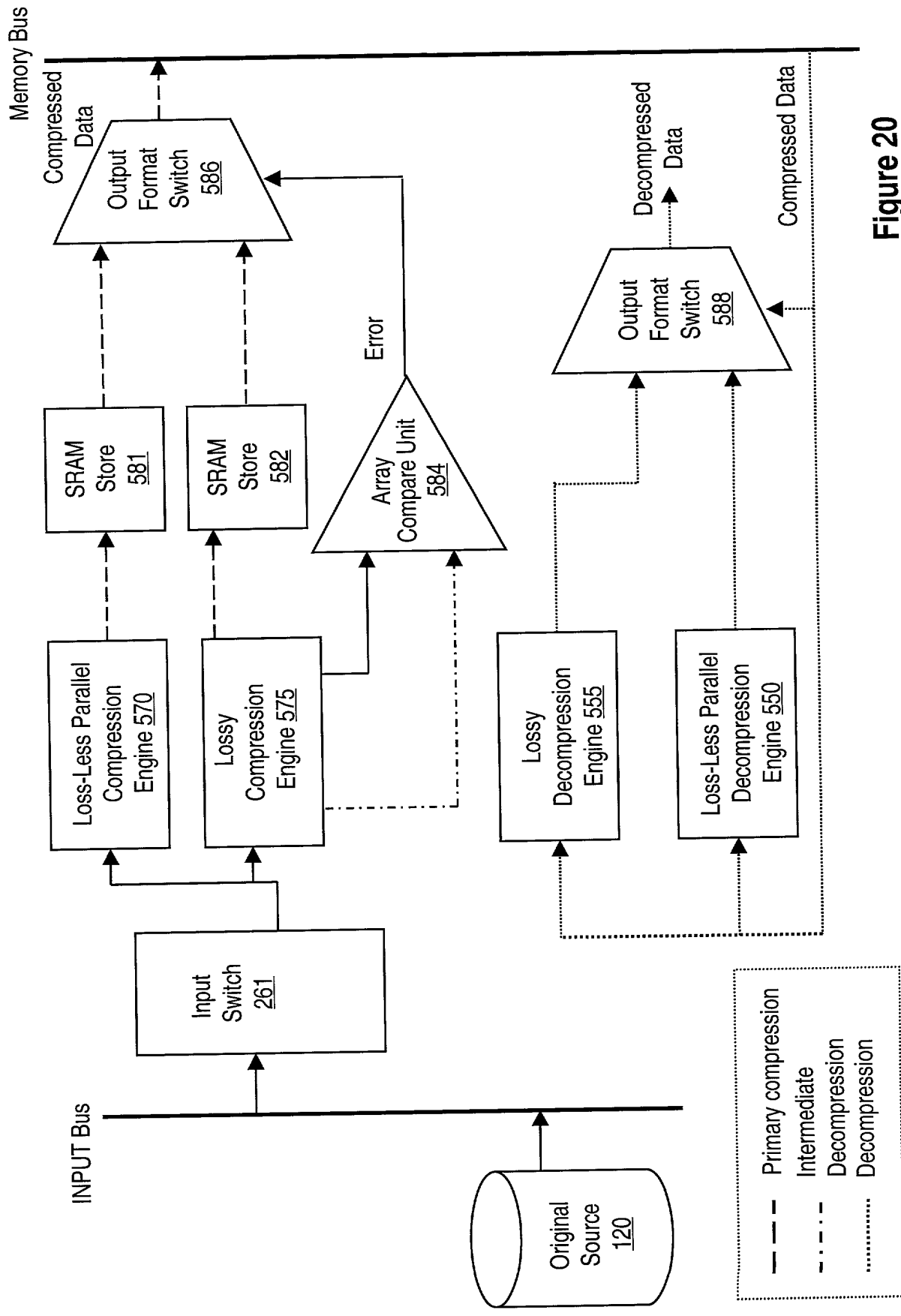


Figure 20



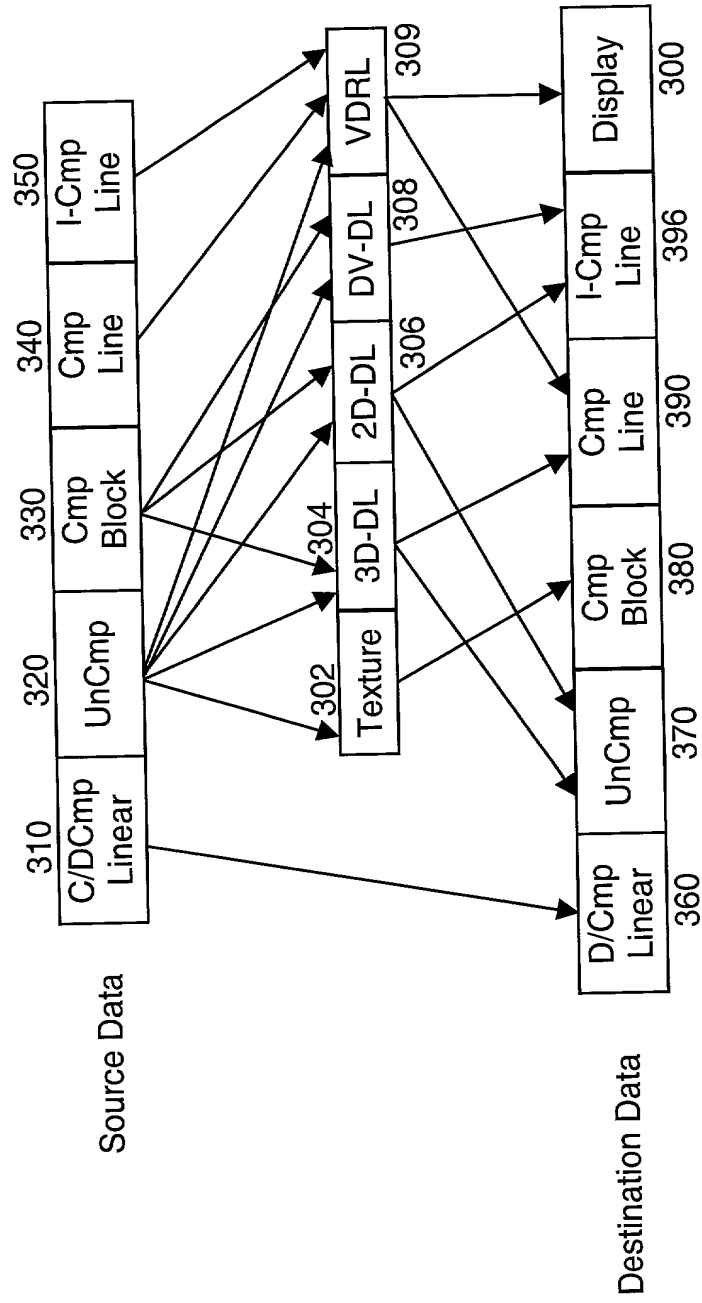
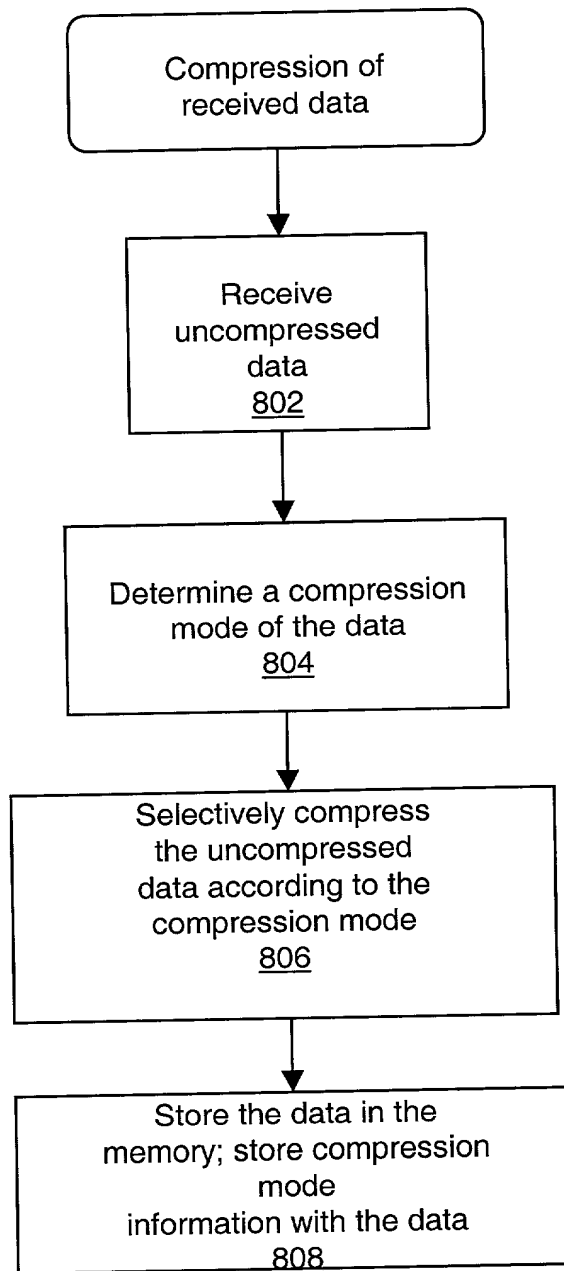
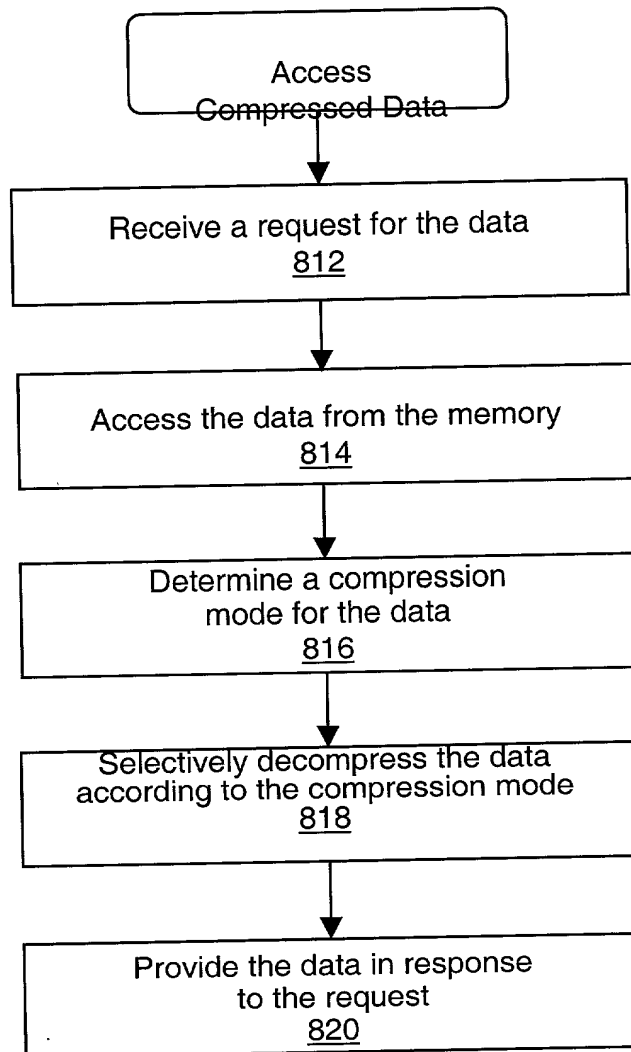


Figure 21

**Figure 22**

**Figure 23**

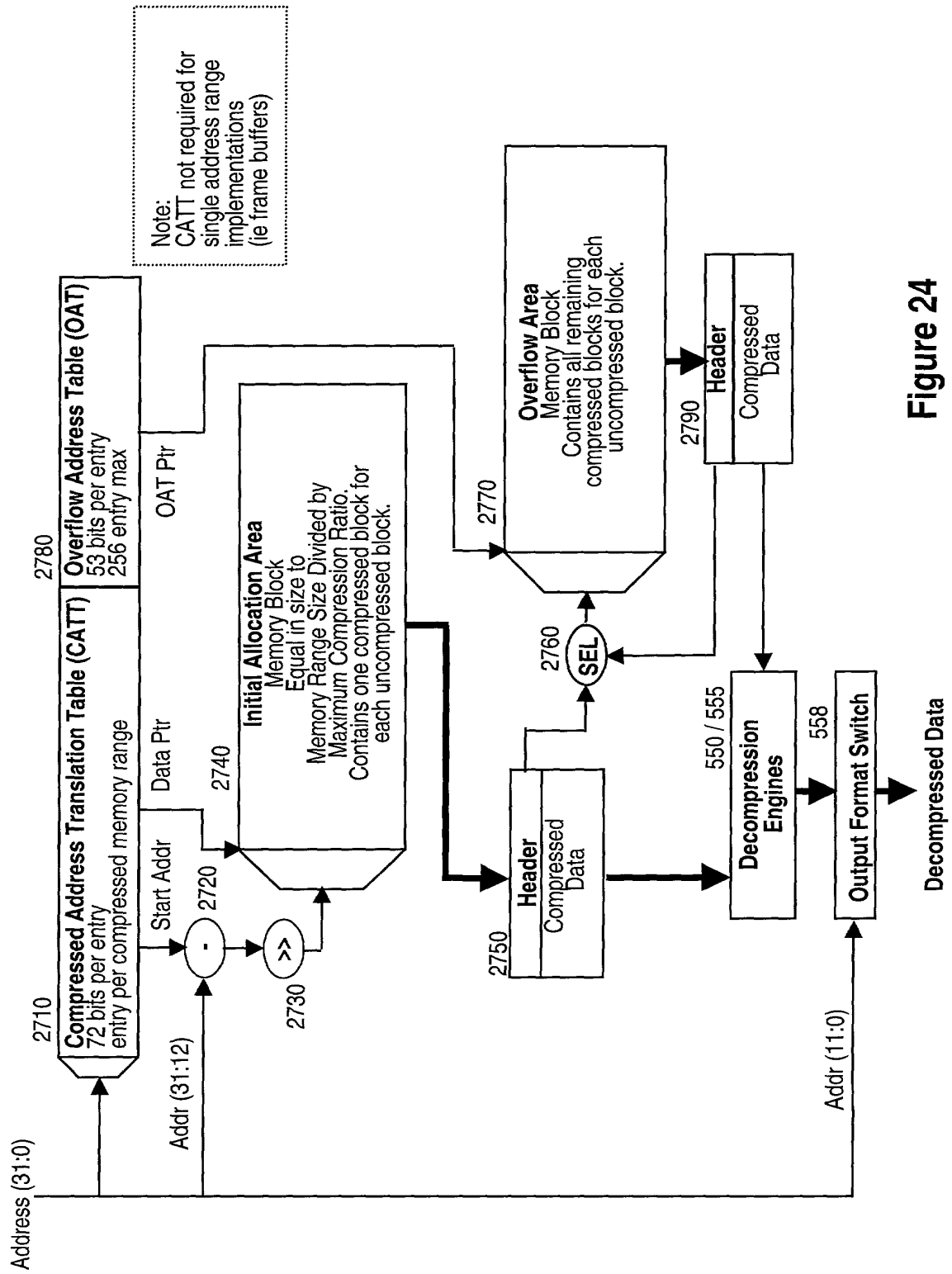


Figure 24

### Memory Allocation Fields

Compressed Address Translation Table (CATT) – 128 Entry Design Limit				
Starting Addr	Ending Addr	Type	Data Ptr	OAT Ptr
20 bits	20 bits	4 bits	20 bits	8 bits
4GB Addressability		Compressed		
4K Boundry	4K Boundry	Blk Size	4K Boundry	4K Boundry
Overflow Address Table (OAT) – 256 Entry Max				
Overflow Ptr	Next Block Ptr	Next OAT Ptr		Next OAT Valid
20 bits	24 bits	8 bits		1 bit
4 GB Addressability		Points to next entry		
4K Boundry		in this table		
Initial Header Description				
Value	# of bits	Meaning		
0	1	Last Block/Unused		
10 A (20 bits)	22	The next block is at offset A in the Overflow Area		
11 1A(8+20 bits)	30	The next block is at offset A in the Overflow Area of OAT entry 1		
Overflow Header Description				
Value	# of bits	Meaning		
00	2	Last Block/Unused		
01	2	The next block follows physically after this one		
10A (8 bits)	10	The next block is A blocks before this one (or after?)		
110A (20 bits)	23	The next block is at offset A in the Overflow Area		
111 1A (8+20 bits)	31	The next block is at offset A in the Overflow Area of OAT entry 1		

Figure 25

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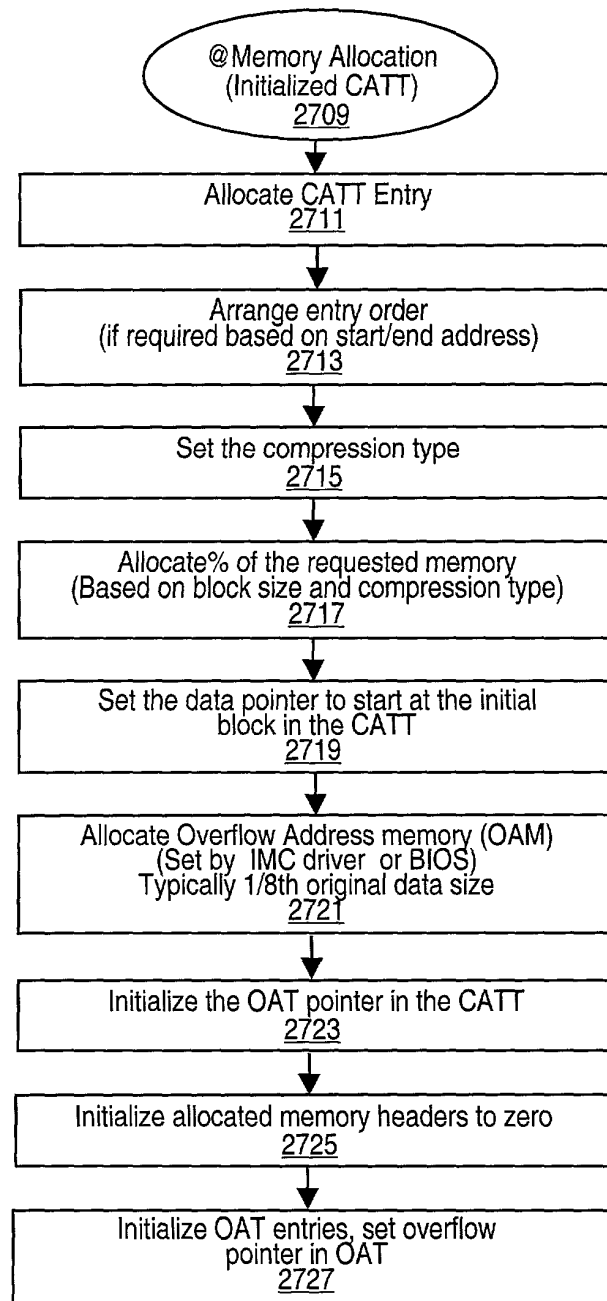


Figure 26

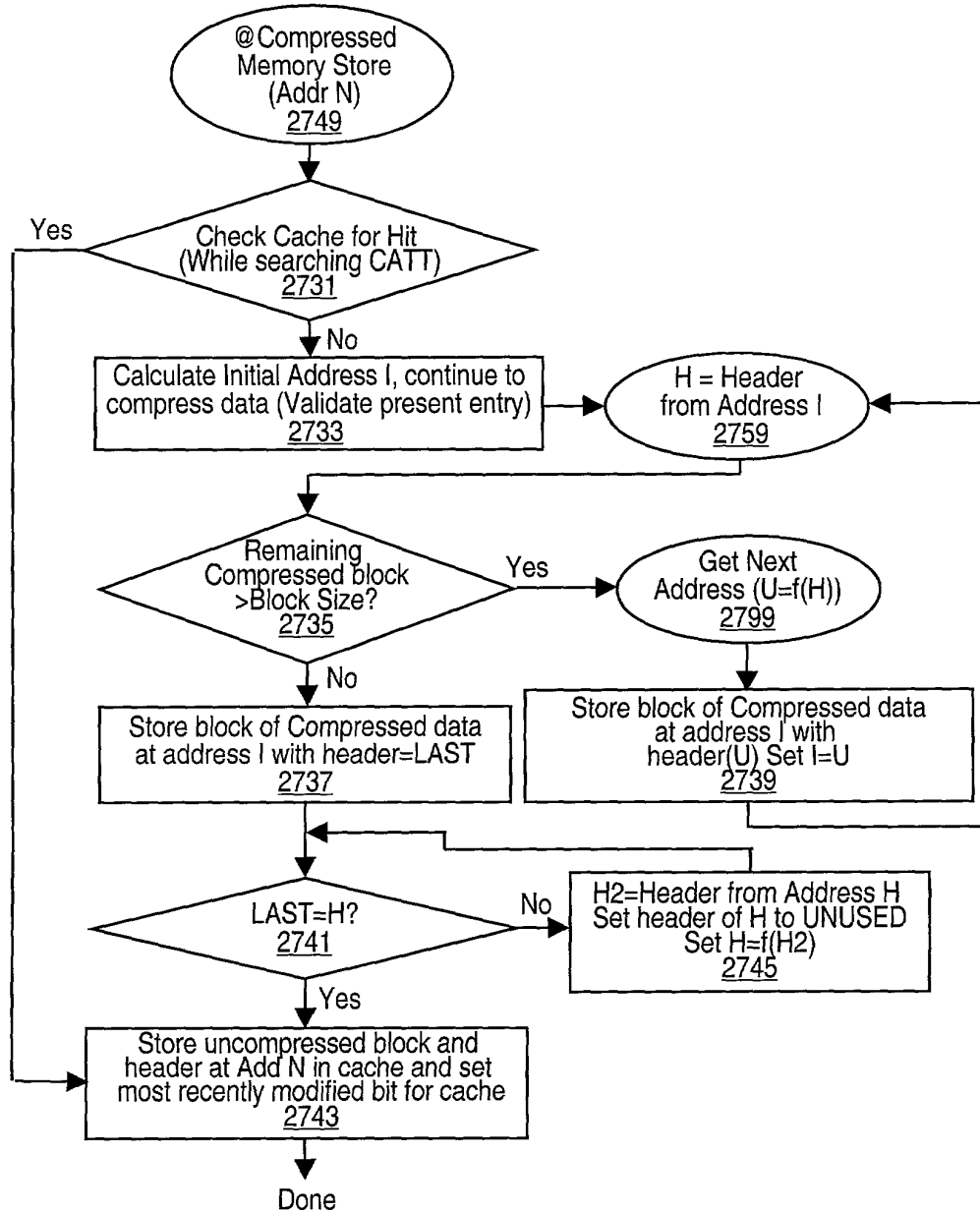


Figure 27

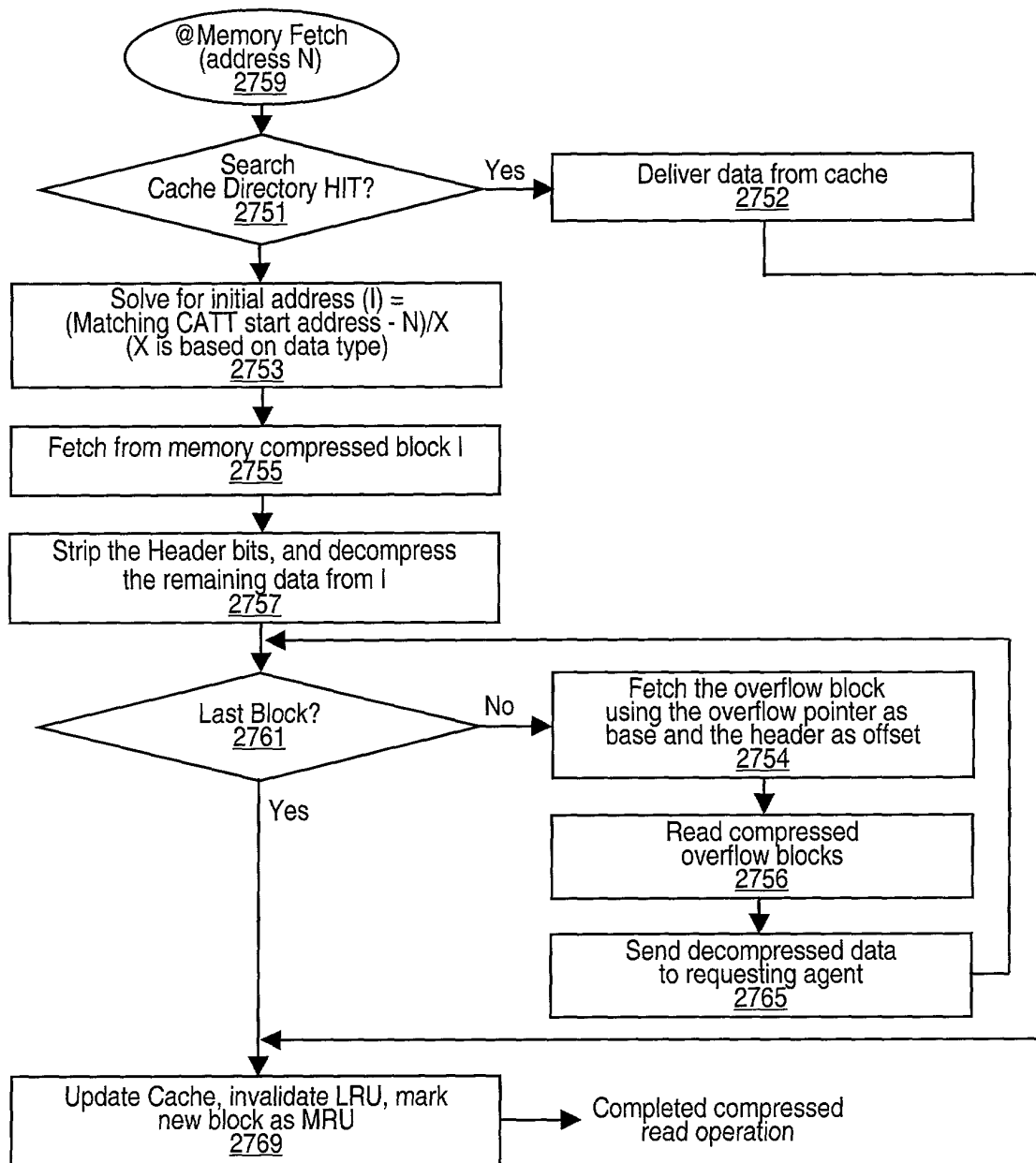


Figure 28



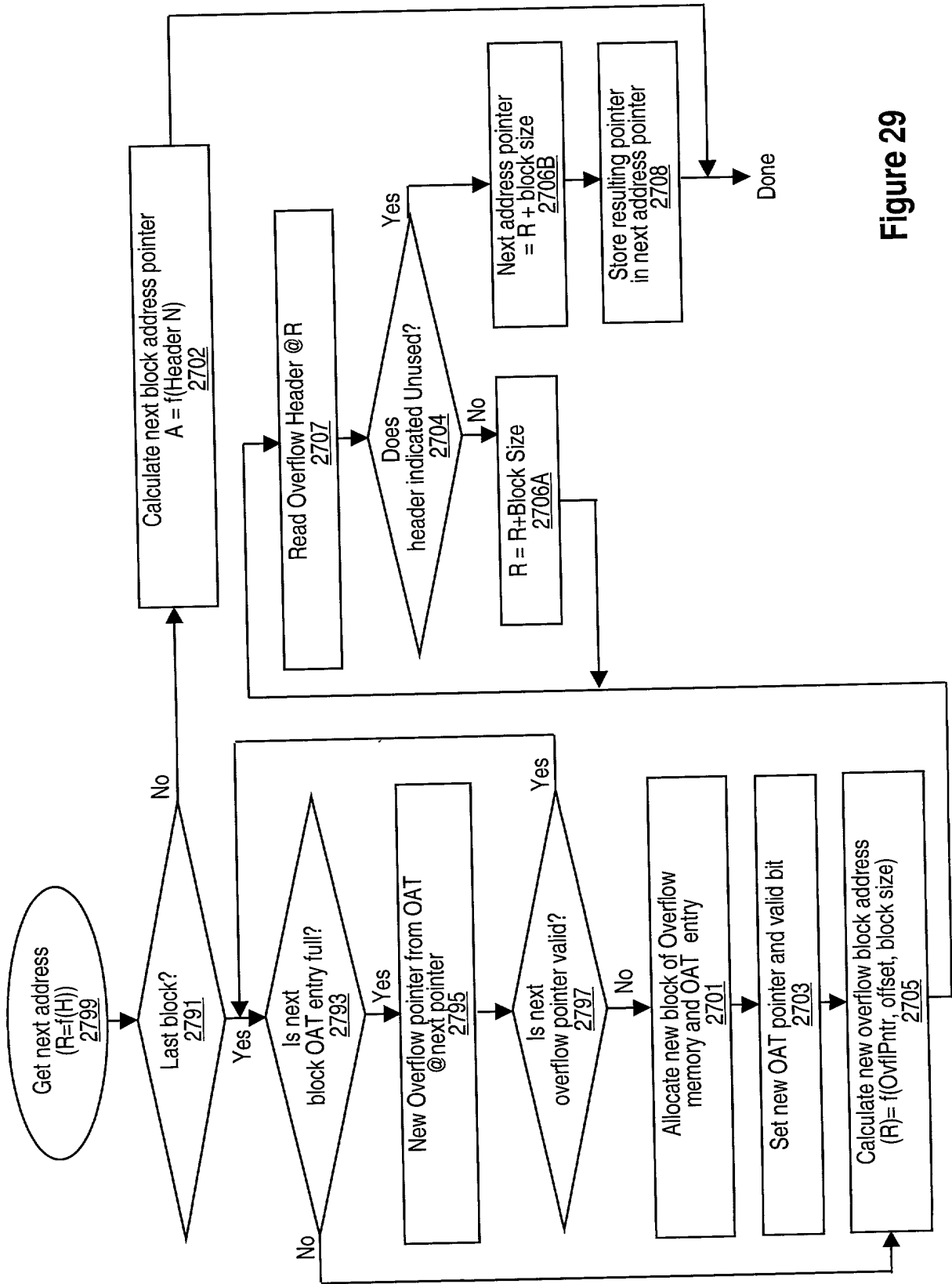
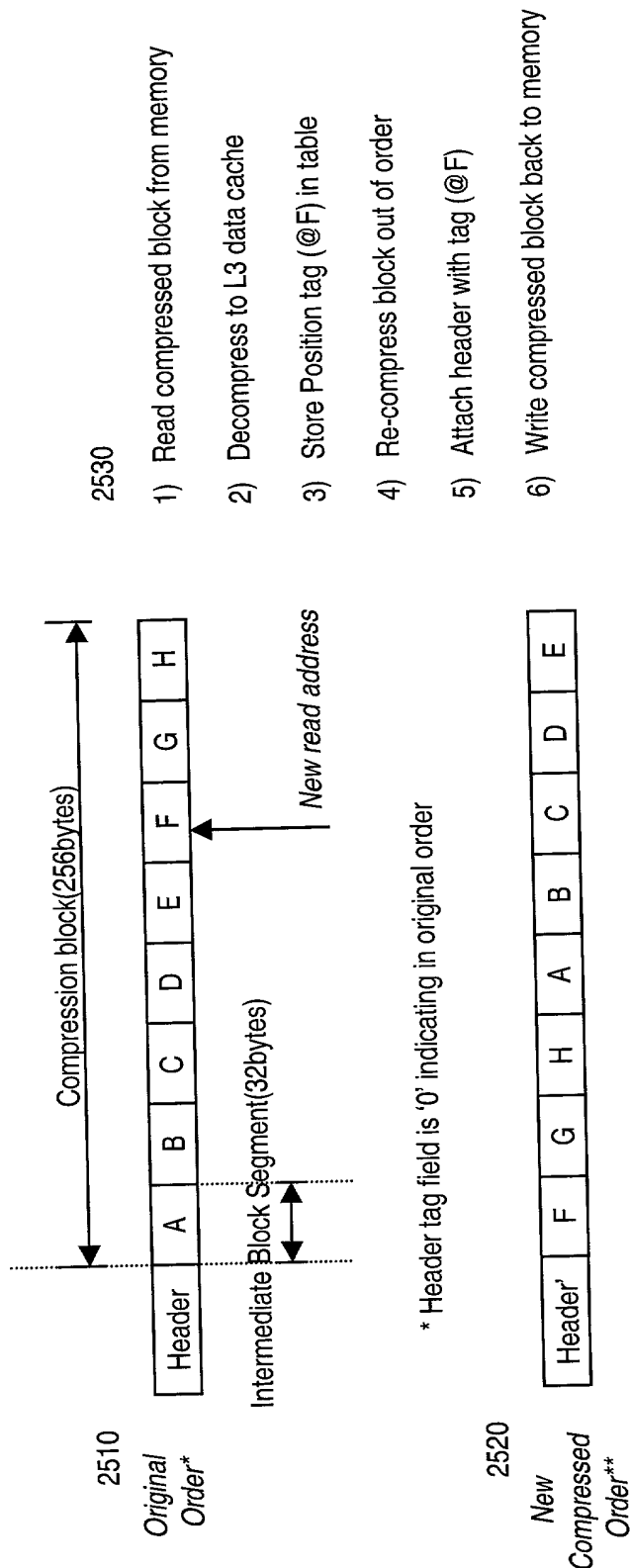


Figure 29

### Figure 30



\* Header tag field is '0' indicating in original order

Figure 31

\*\* Header tag field is '5' indicating out of order

Bytes Compressed	Flag	Index	Count	Data	Bits Used
0	0	-	-	8b	9
1	10	6b	-	-	8
2	1100	6b	-	-	10
3	1101	6b	-	-	10
4	1110	6b	-	-	10
5	1111000	6b	-	-	13
6	1111001	6b	-	-	13
7	1111010	6b	-	-	13
8	1111011	6b	-	-	13
9	1111100	6b	-	-	13
10	1111101	6b	-	-	13
11	1111110	6b	-	-	13
>11	1111111	6b	12b	-	25

Figure 32

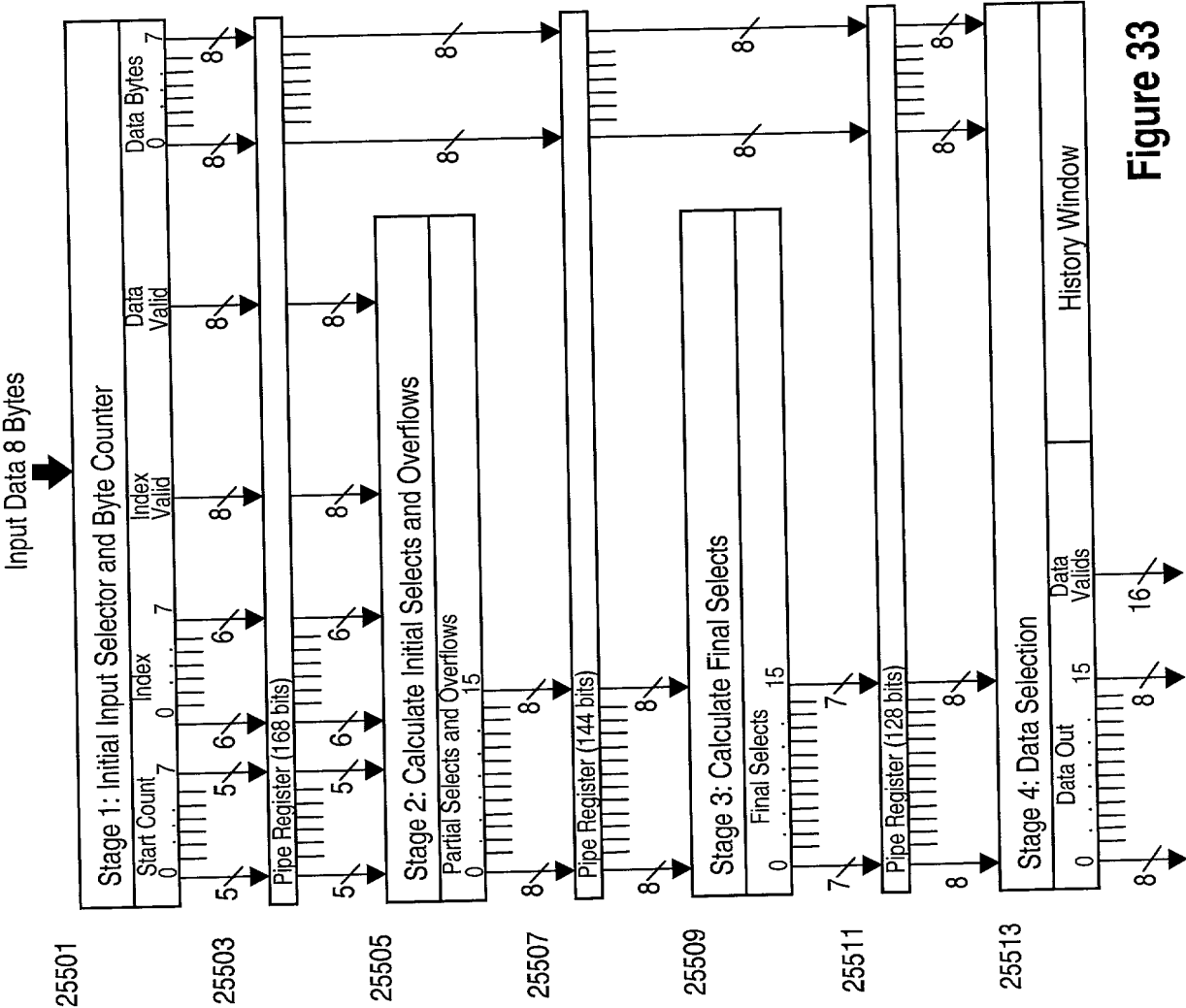


Figure 33

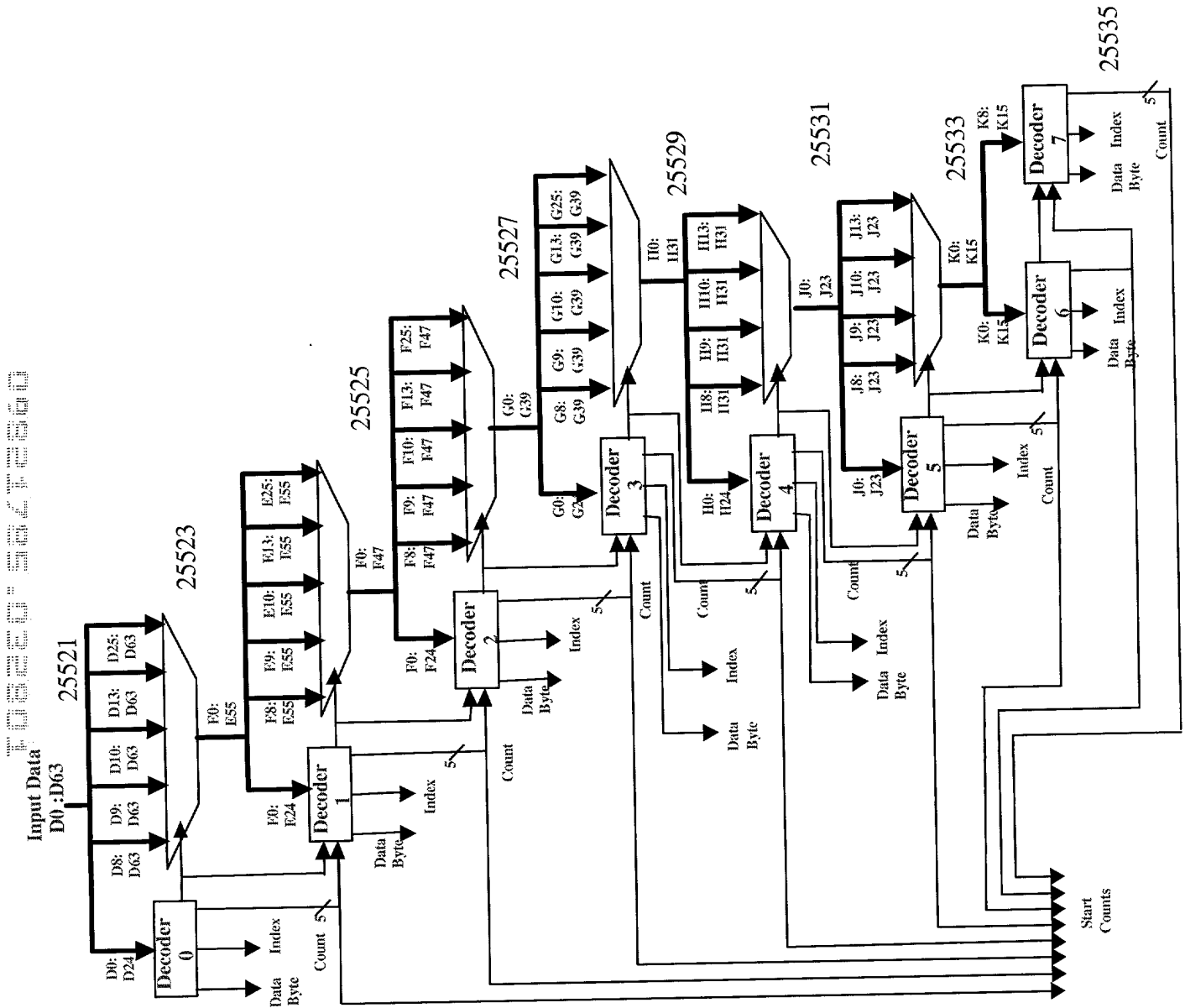


Figure 34

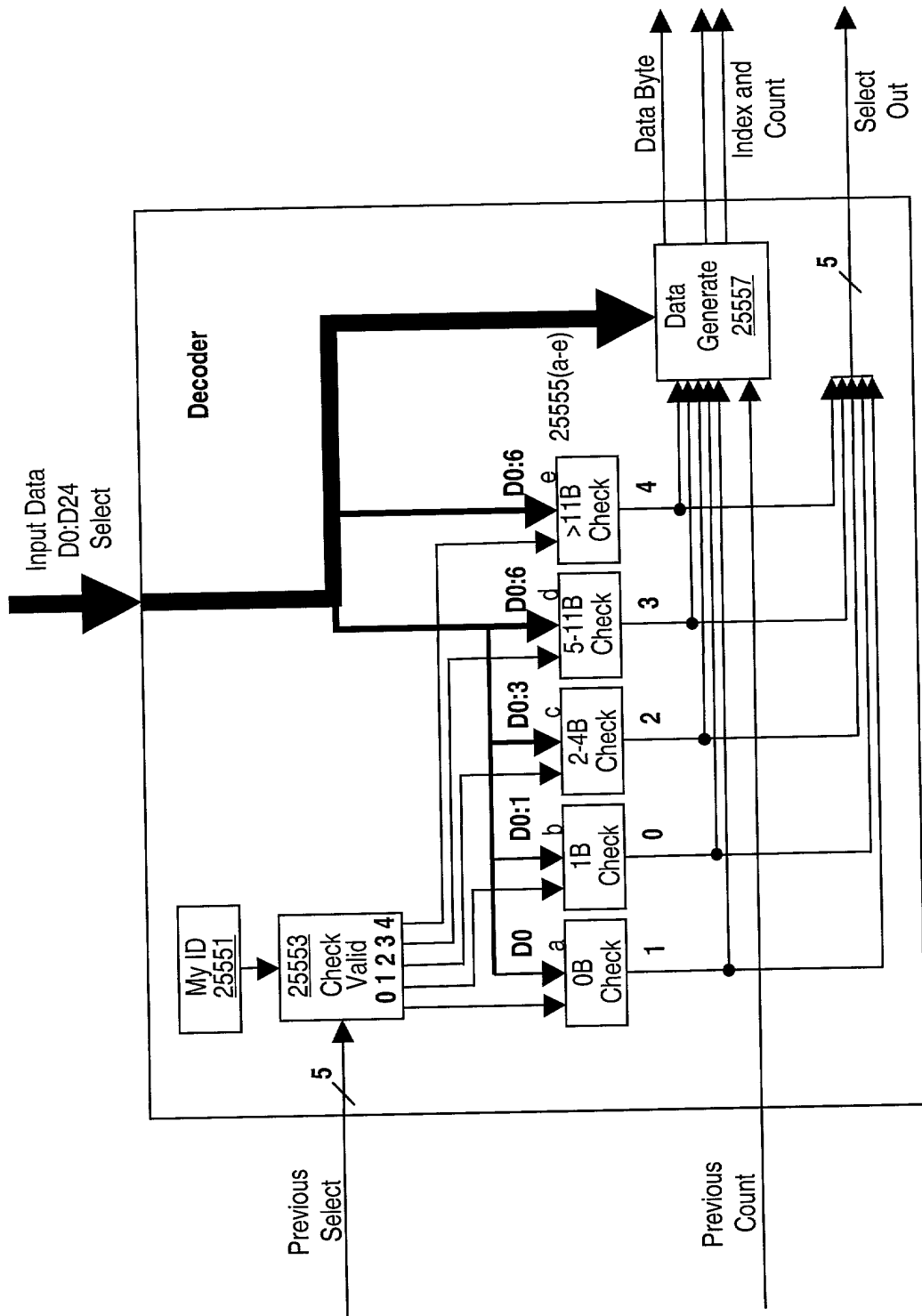


Figure 35

Previous Select	10	08	04	02	01	00
My ID=01	1F	1F	1F	1F	1F	00
My ID=02	1F	1F	1F	1F	1F	00
My ID=04	1F	1F	1F	1F	1F	00
My ID=08	1F	1F	1F	1F	1E	00
My ID=10	1F	1F	1F	1F	1E	00
My ID=20	1E	1E	1E	1E	00	00
My ID=40	1E	1E	1E	1C	00	00
My ID=80	08	00	00	00	00	00

Figure 36a

Select	10	08	04	02	01	00
Data Byte	X	D1:D8	X	X	X	X
Index	D2:D7	X	D4:D9	D7:D12	D7:D12	X
Count	PC+1	PC+1	D2:D3+PC+2	D4:D6+PC+5	D13:D24+PC	X

Figure 36b



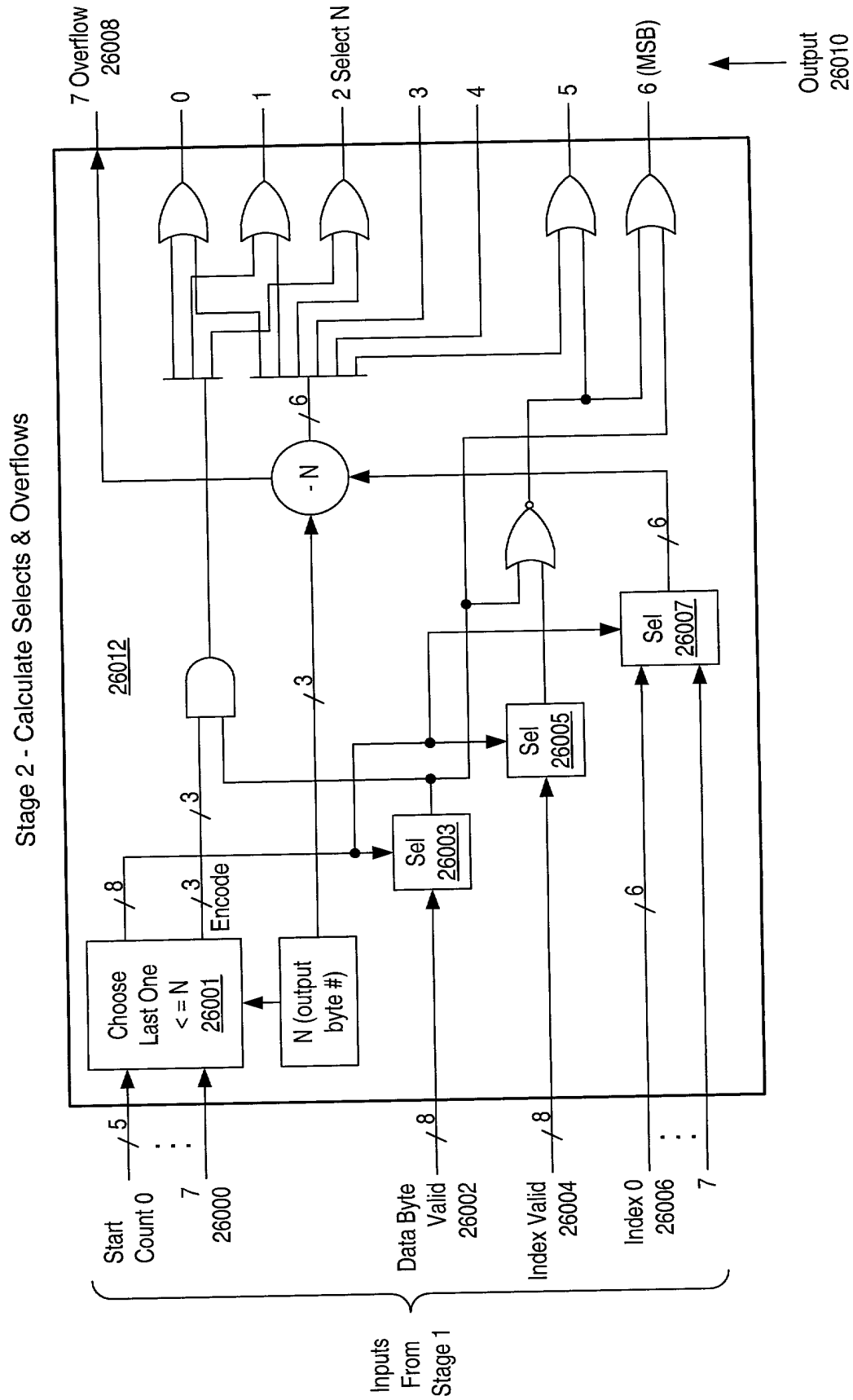
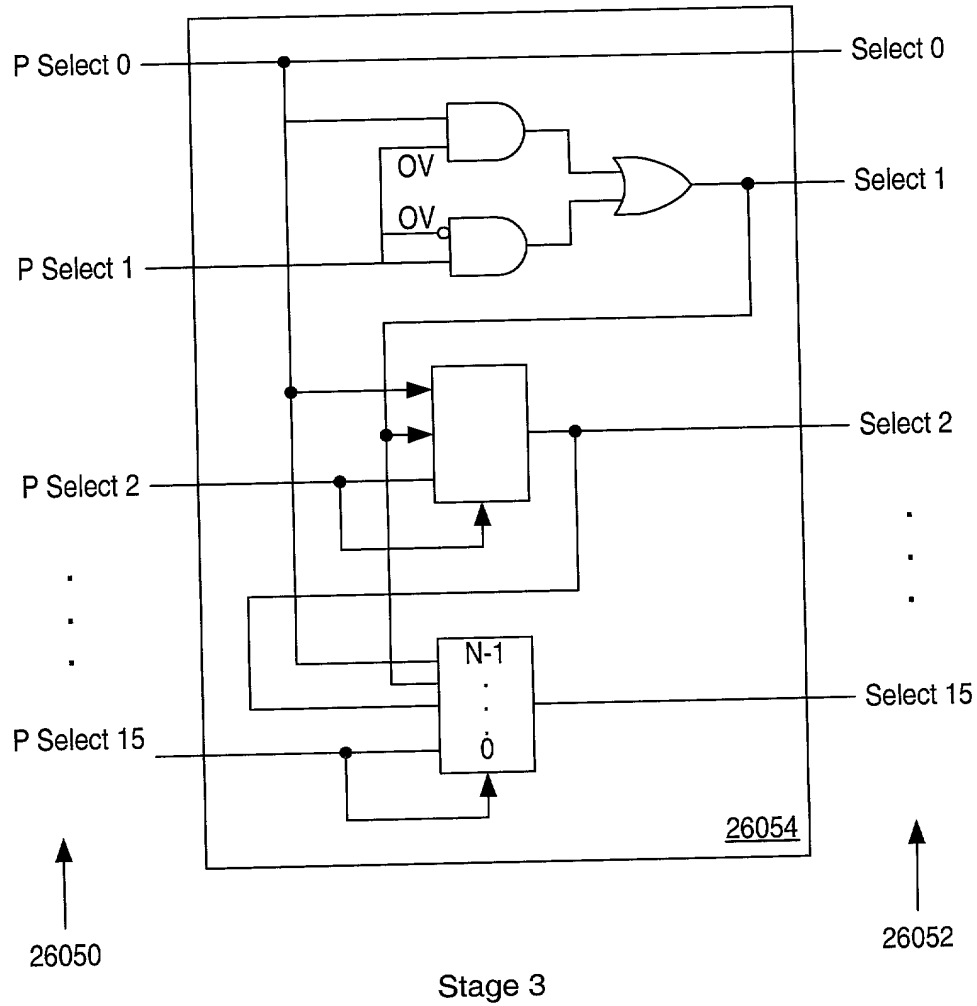


Figure 37

**Figure 38**

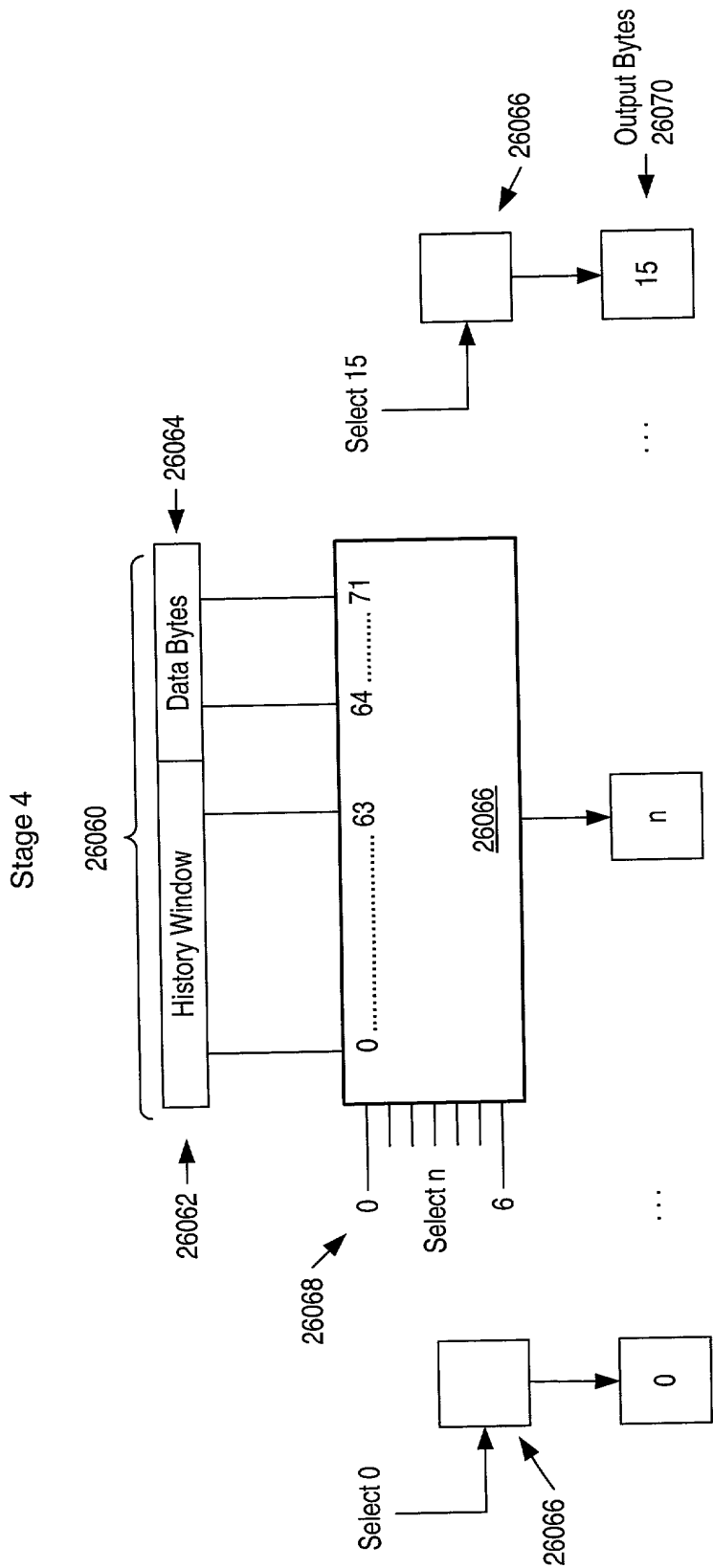
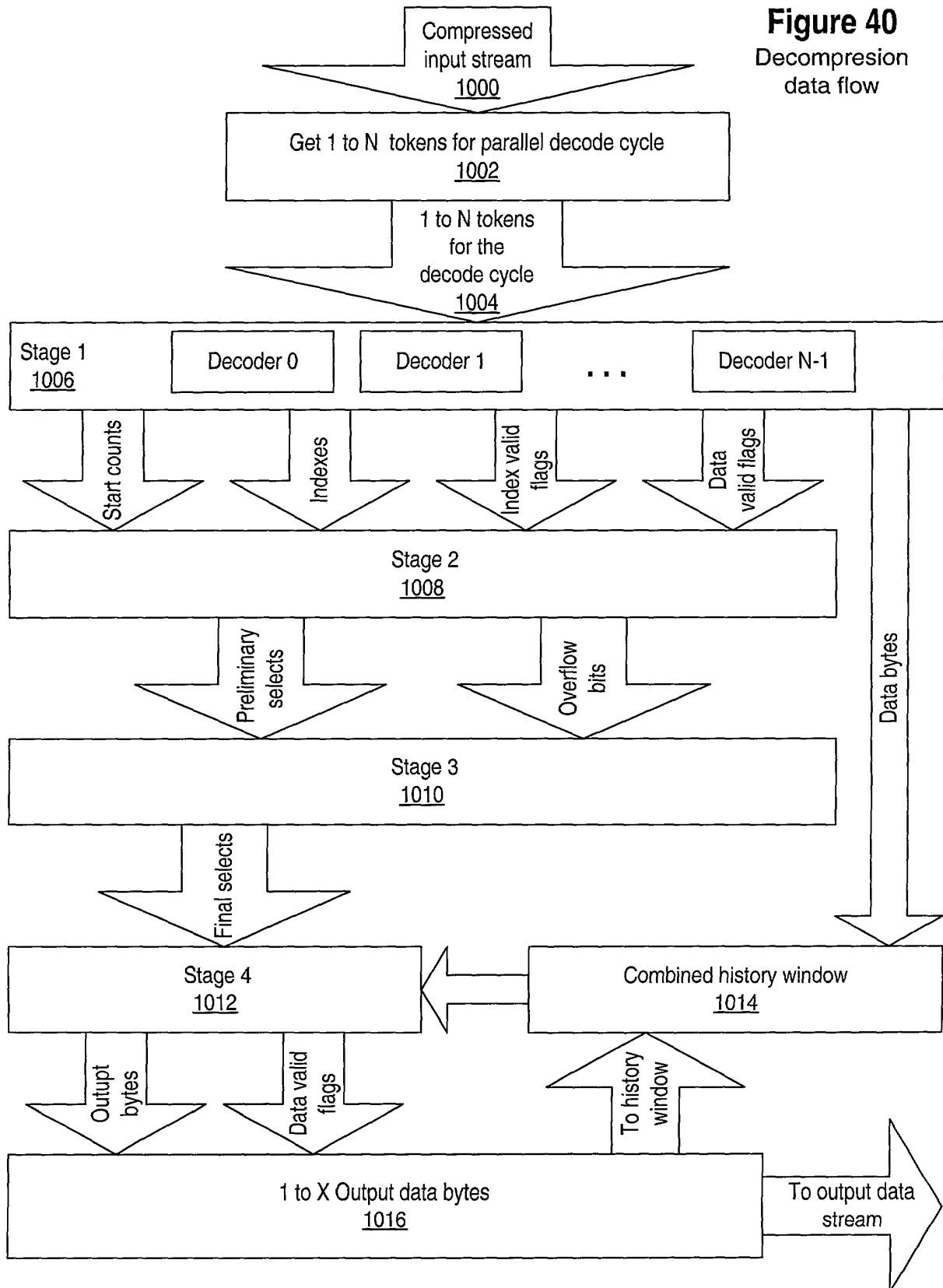
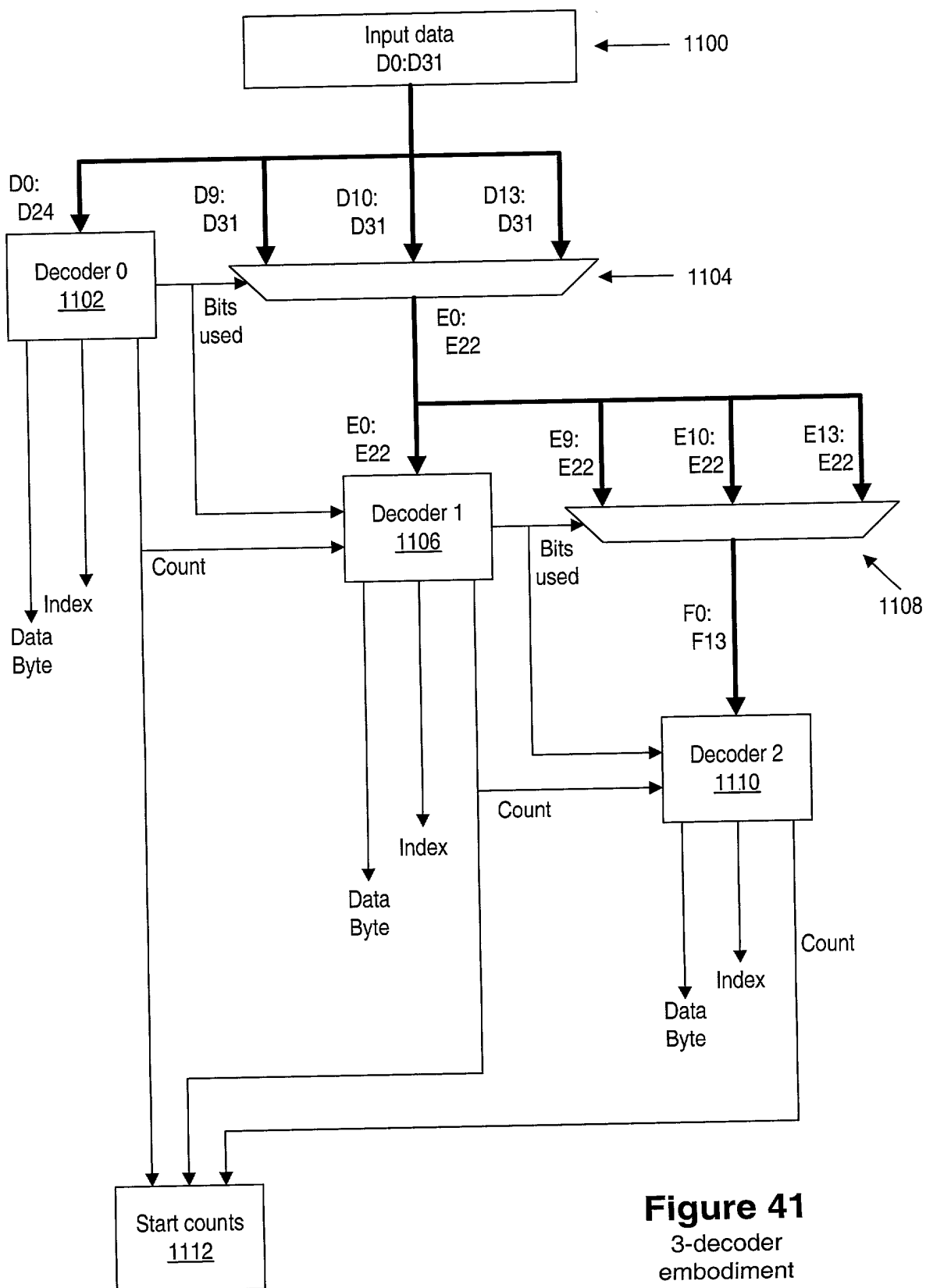


Figure 39

**Figure 40**  
Decompression  
data flow





**Figure 41**  
3-decoder  
embodiment

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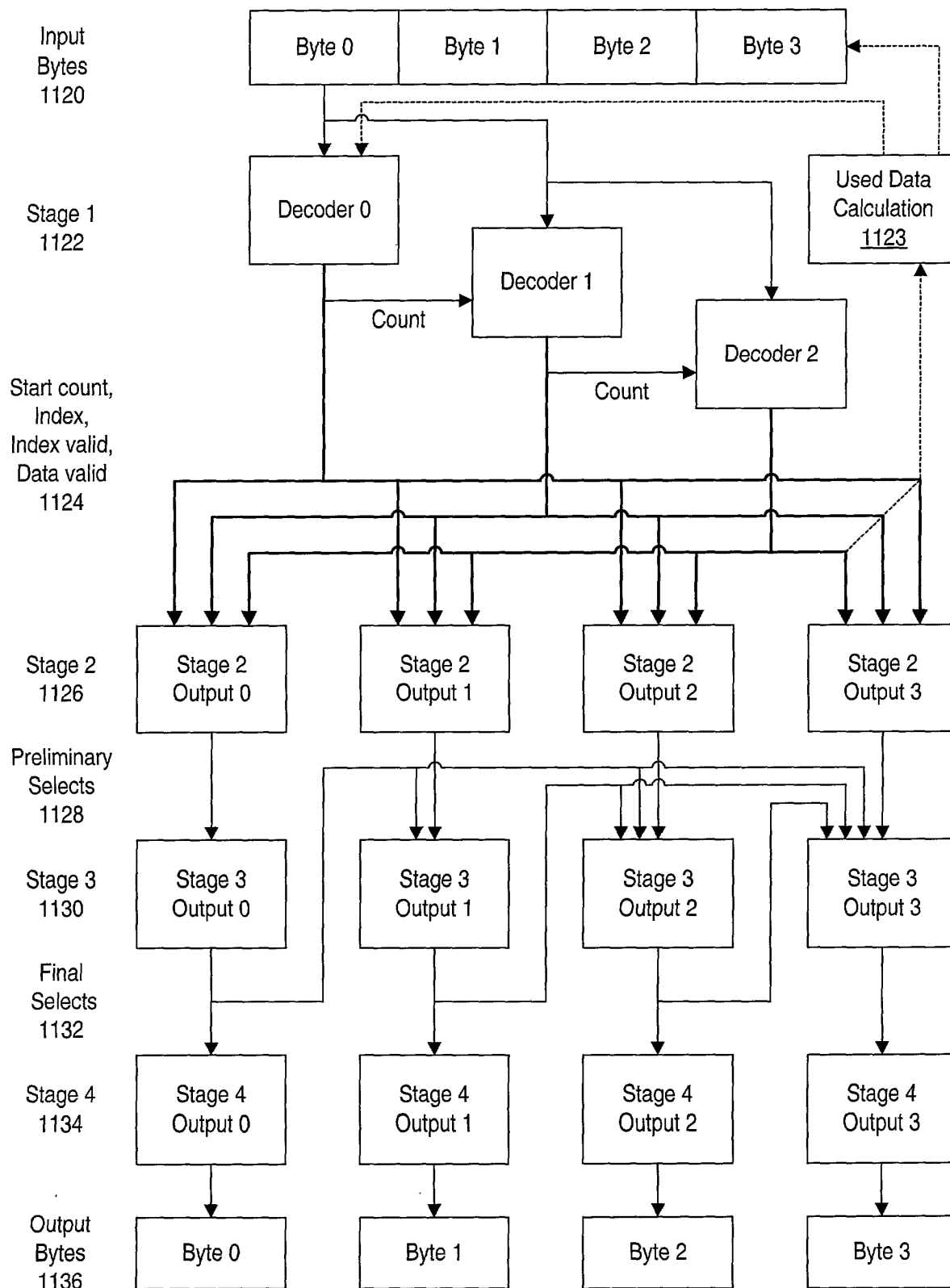
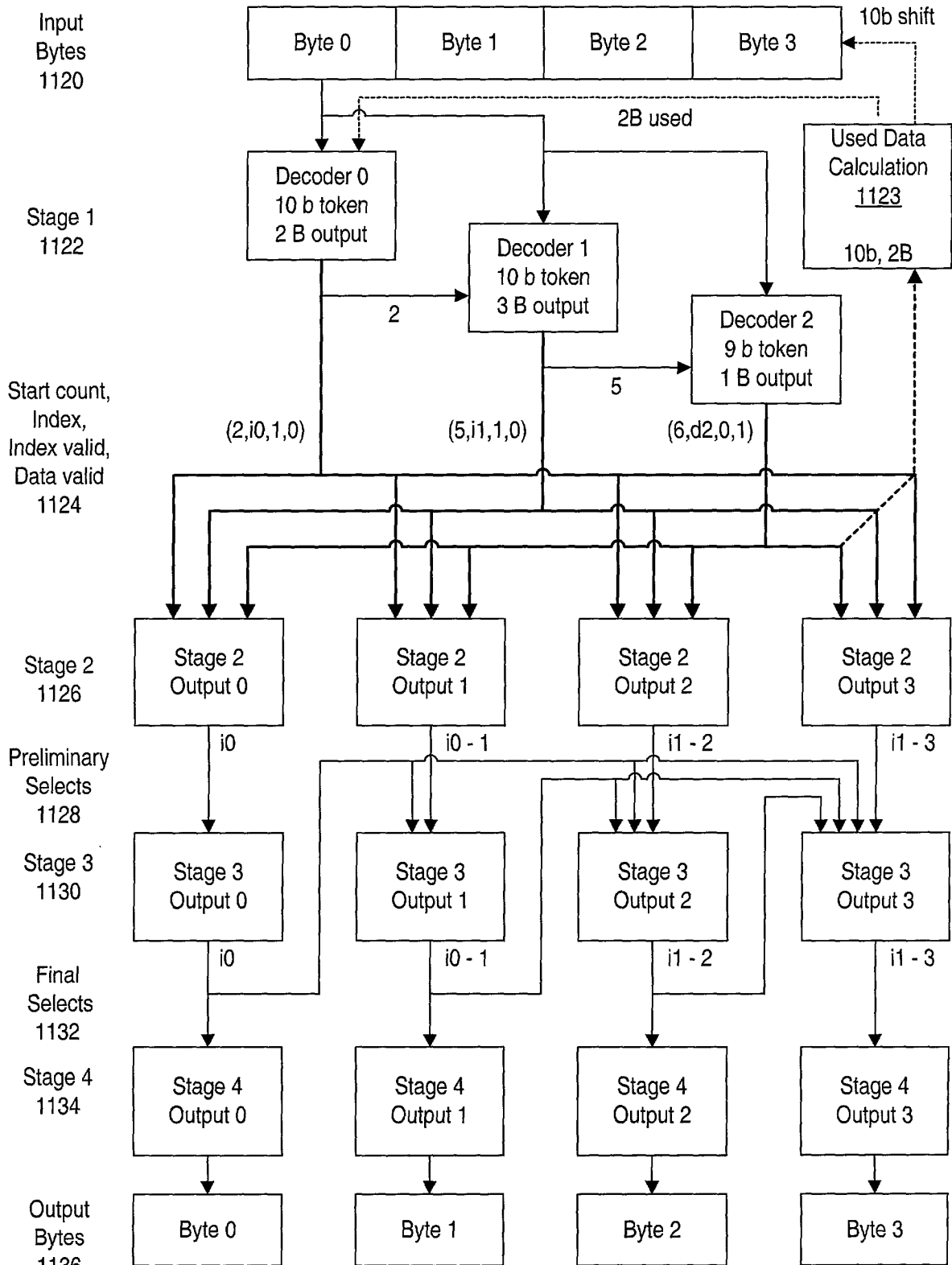


Figure 42a

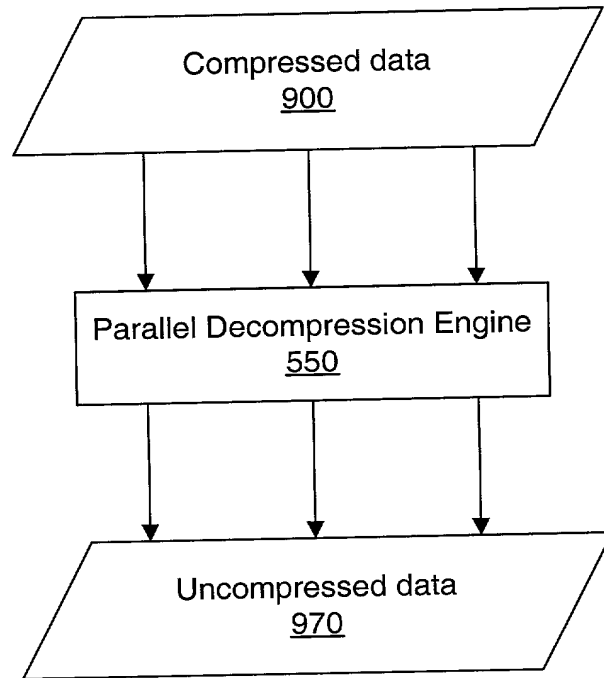
- 4 input bytes, 3 decoders, 4 output bytes

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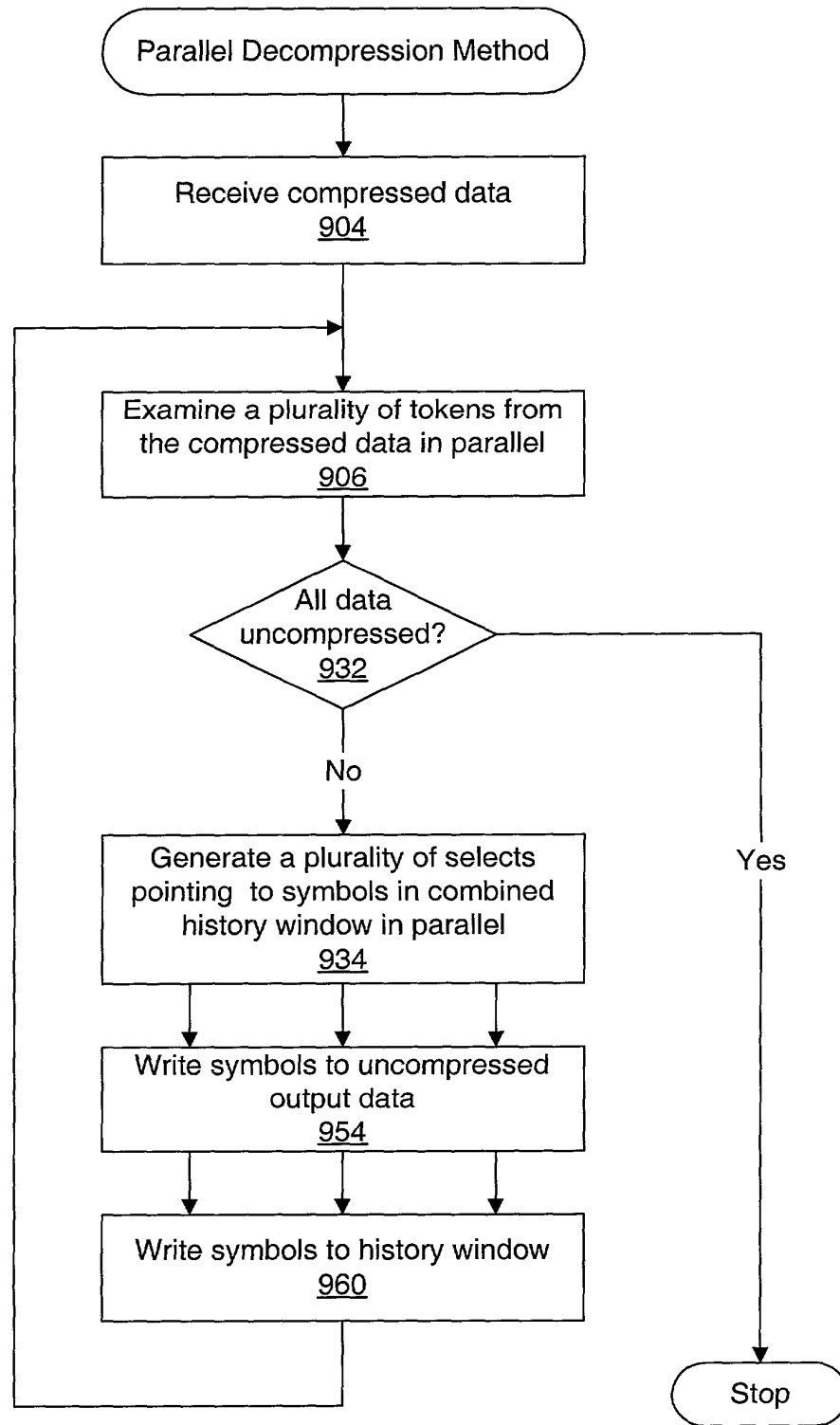
**Figure 42b**

- example using 4 input bytes, 3 decoders, 4 output bytes

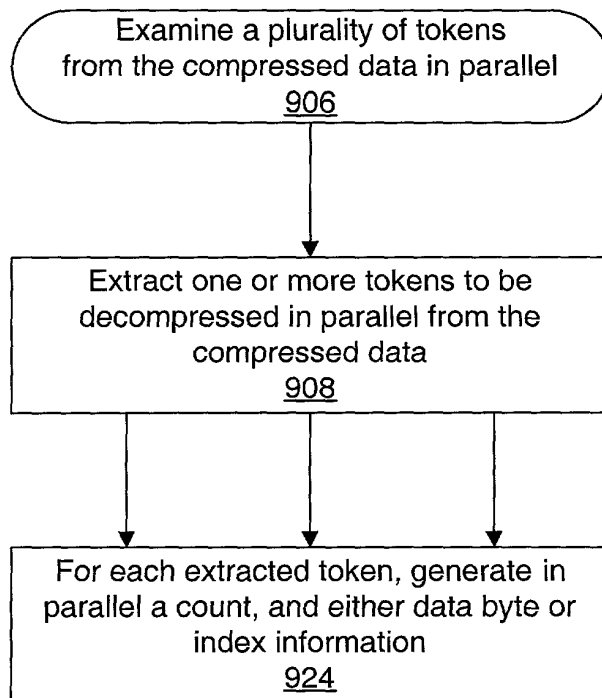


**Figure 43a**  
Decompression  
flowchart

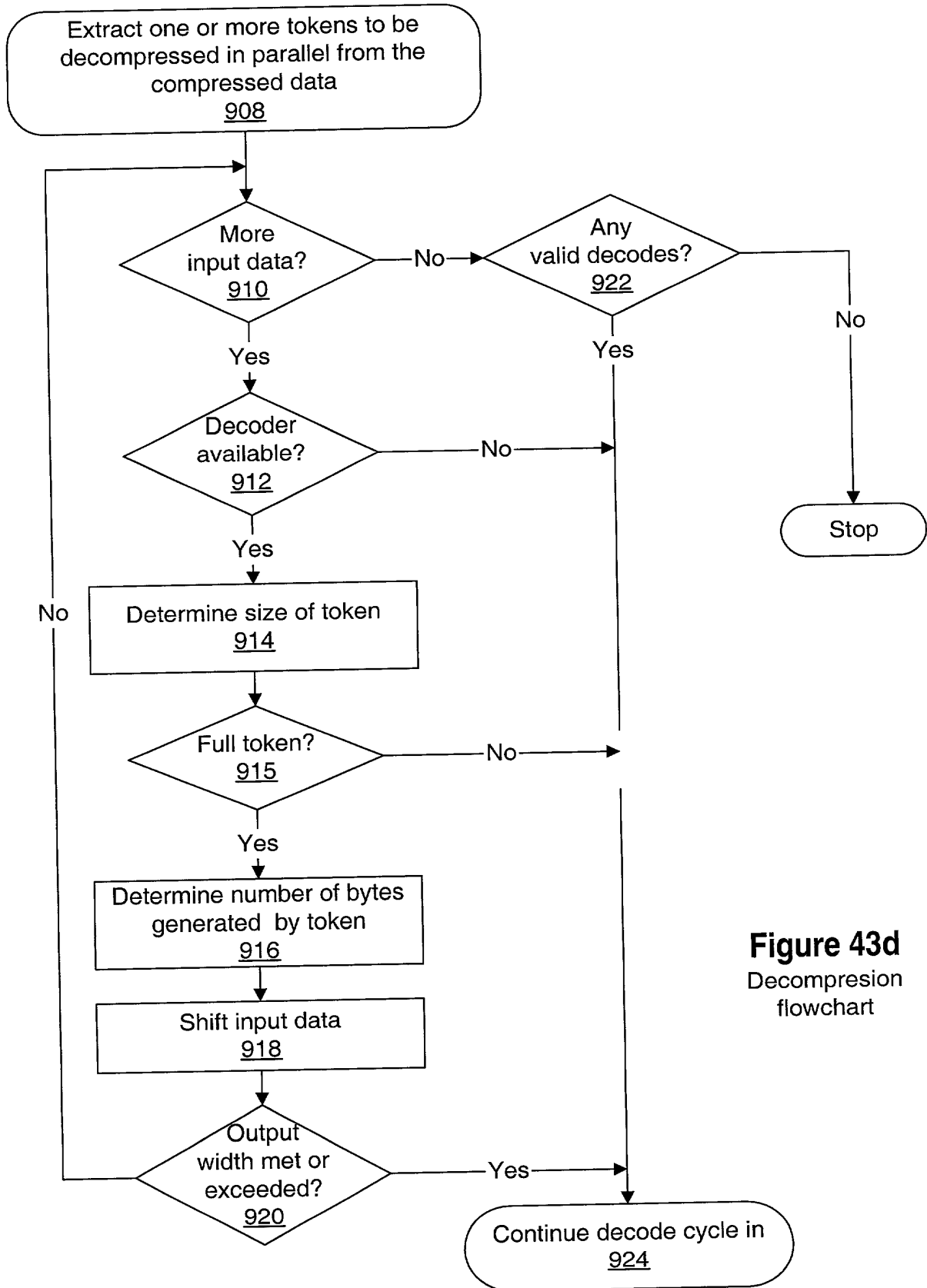


**Figure 43b**

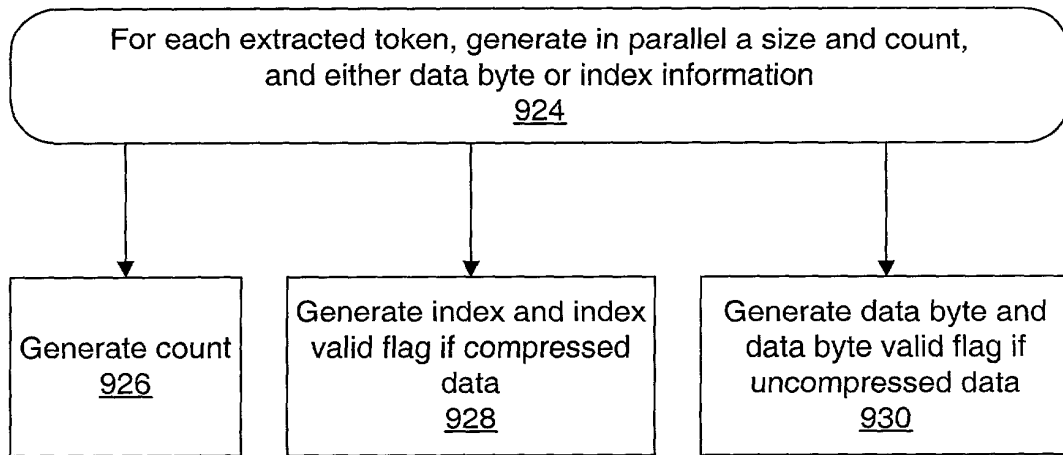
Decompression flowchart

**Figure 43c**

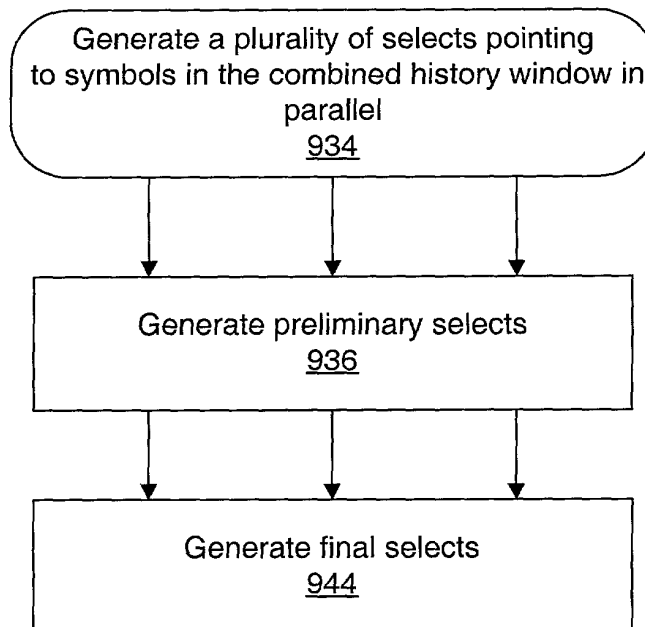
Decompression flowchart



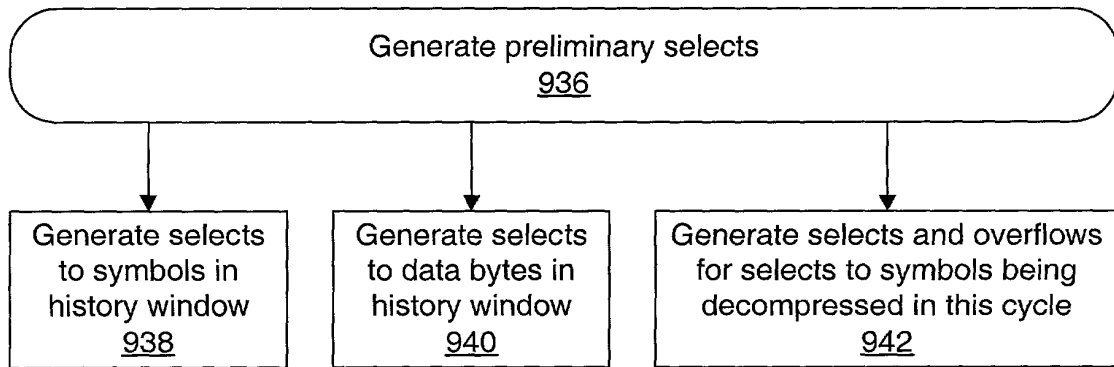
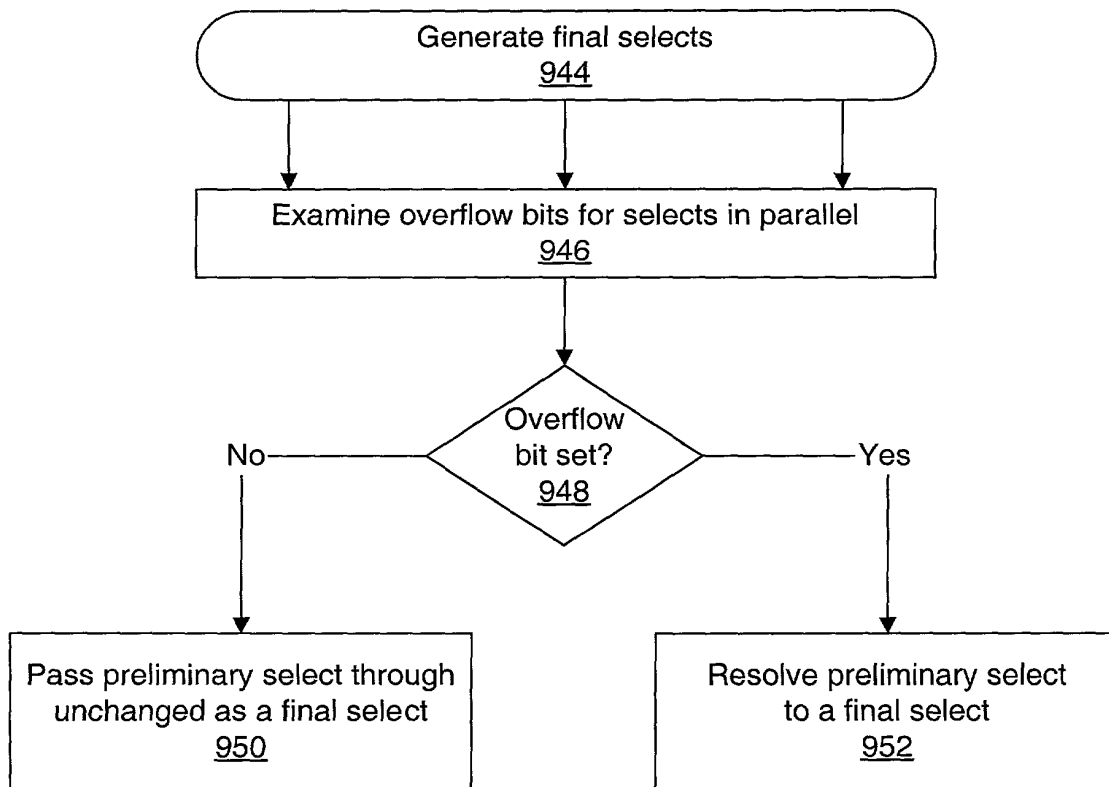
**Figure 43d**  
Decompression  
flowchart

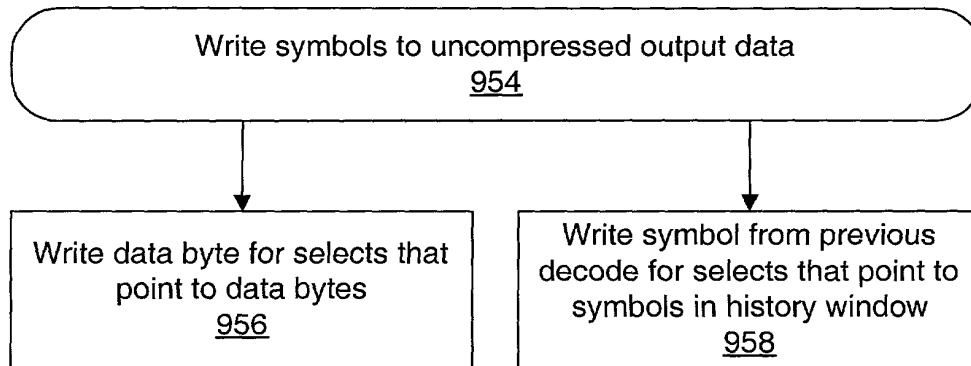


**Figure 43e**  
Decompression flowchart

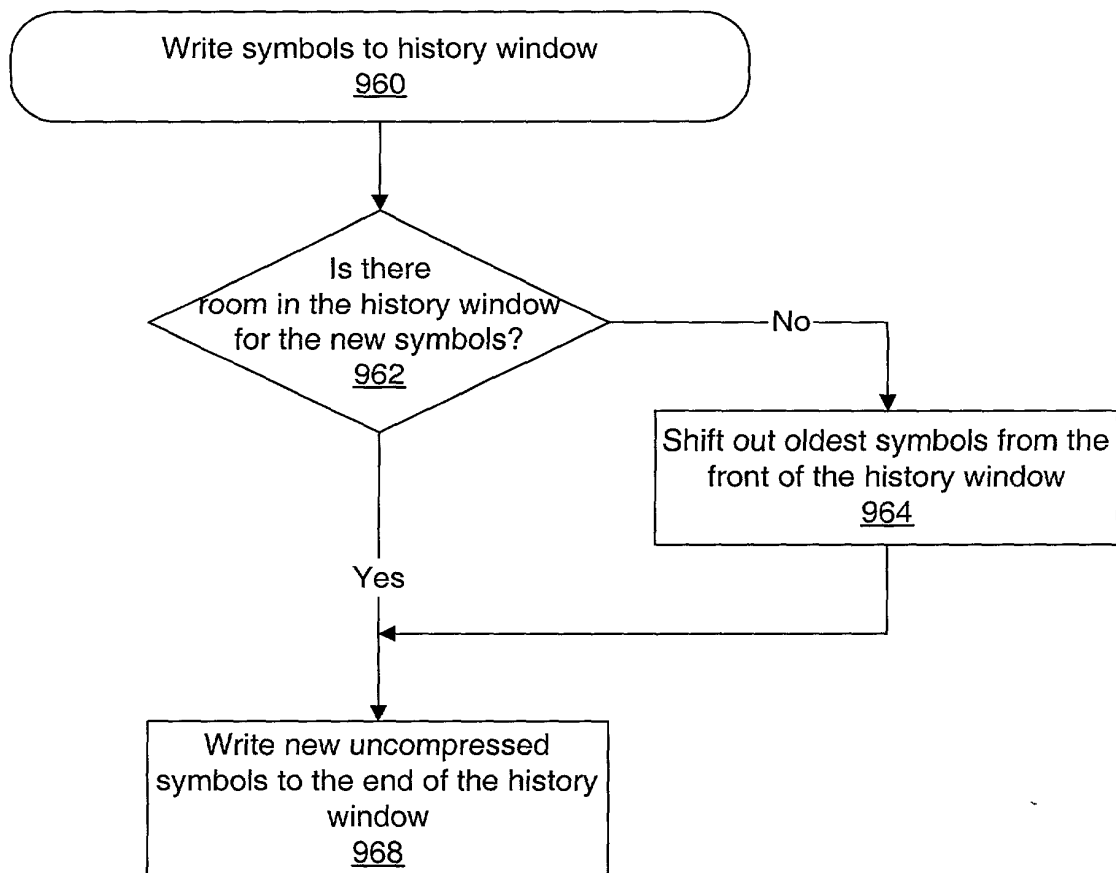


**Figure 43f**  
Decompression flowchart

**Figure 43g**Decompression  
flowchart**Figure 43h**Decompression  
flowchart



**Figure 43i**  
Decompression flowchart



**Figure 43j**  
Decompression flowchart

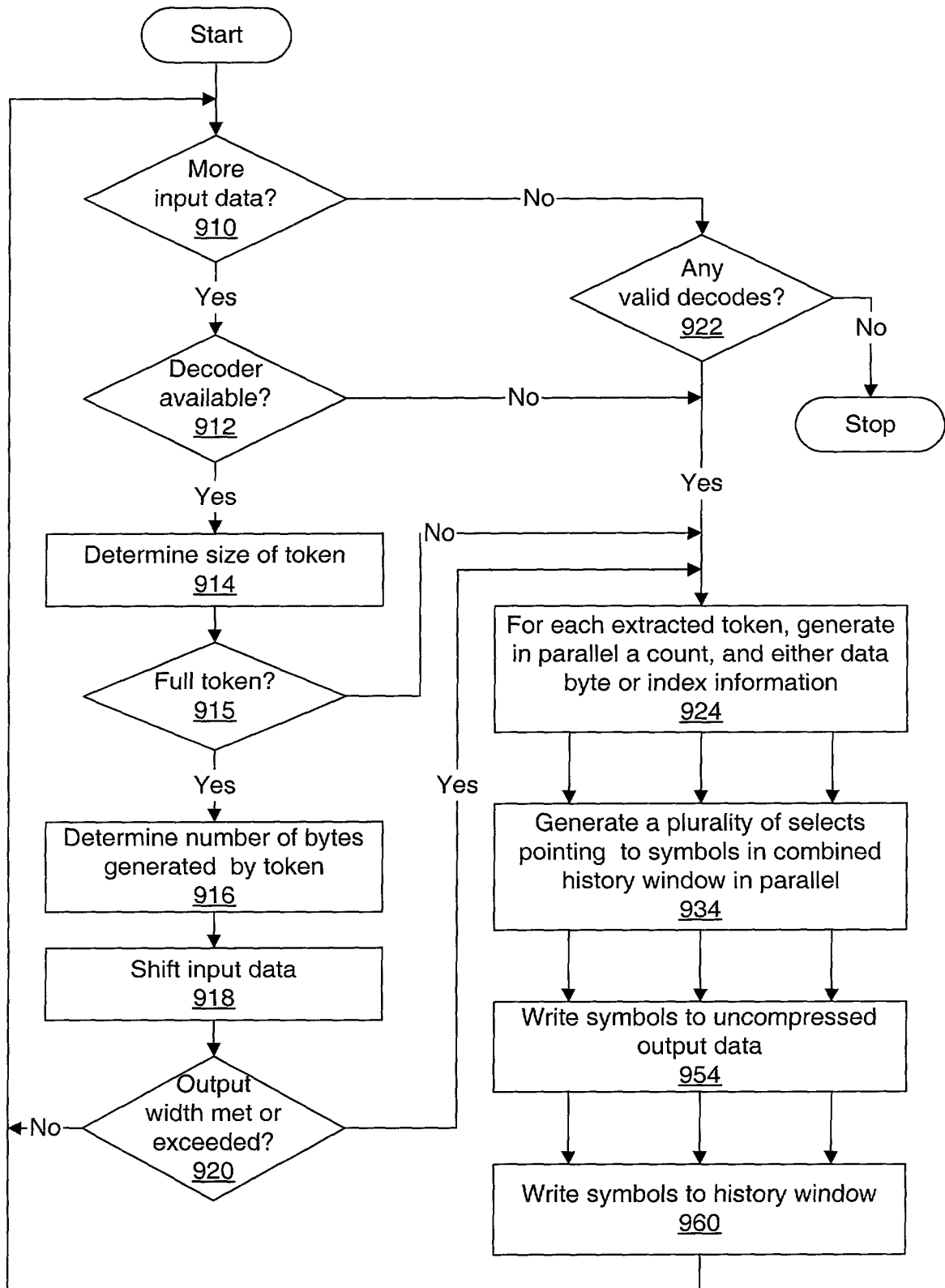


Figure 43k

Decompression flowchart

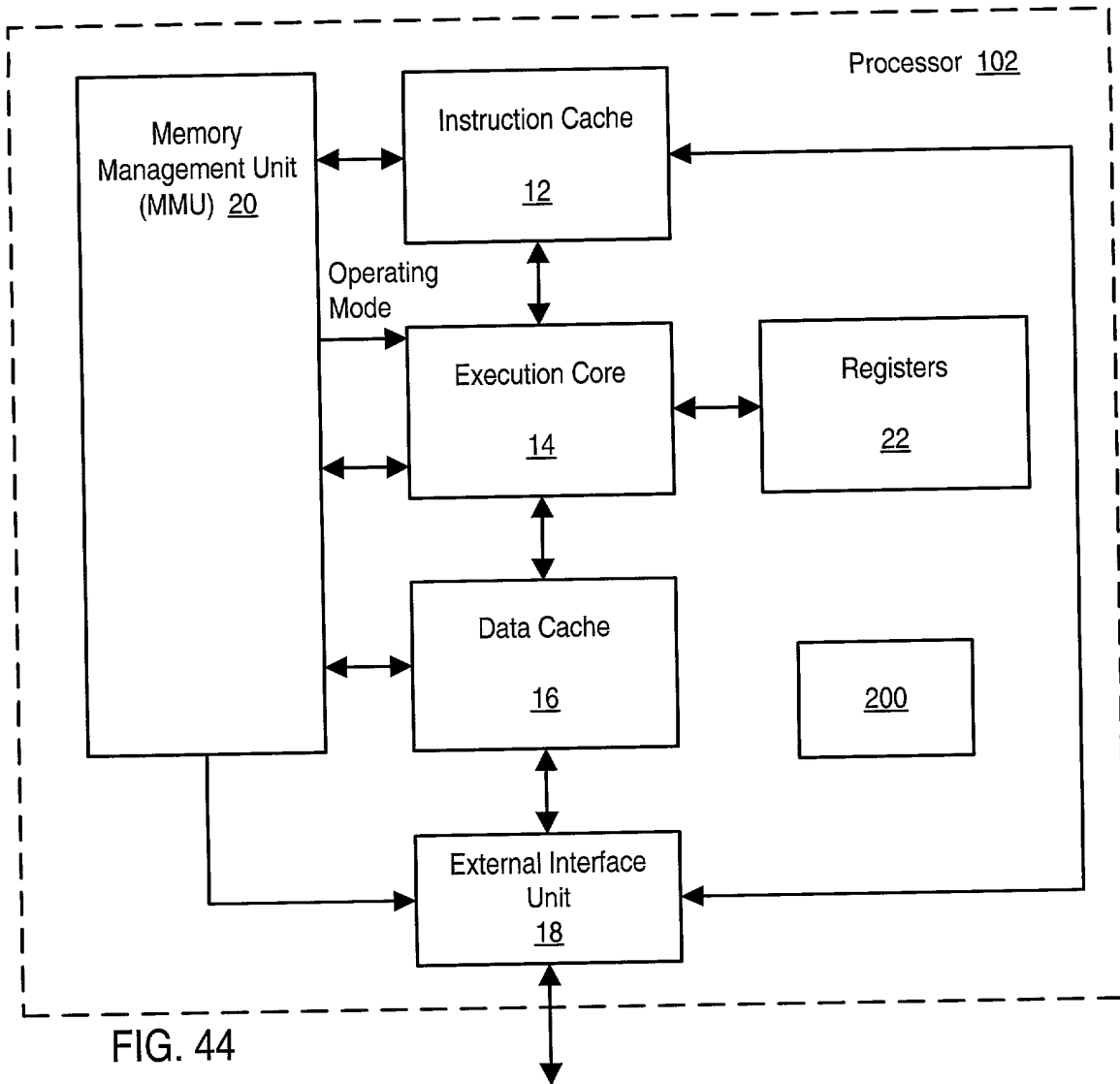
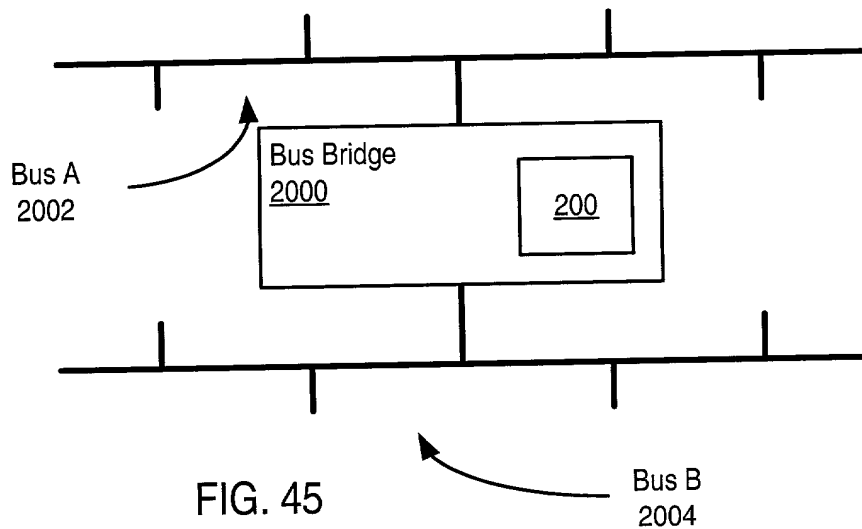


FIG. 44

FIG. 45  
Bus Bridge



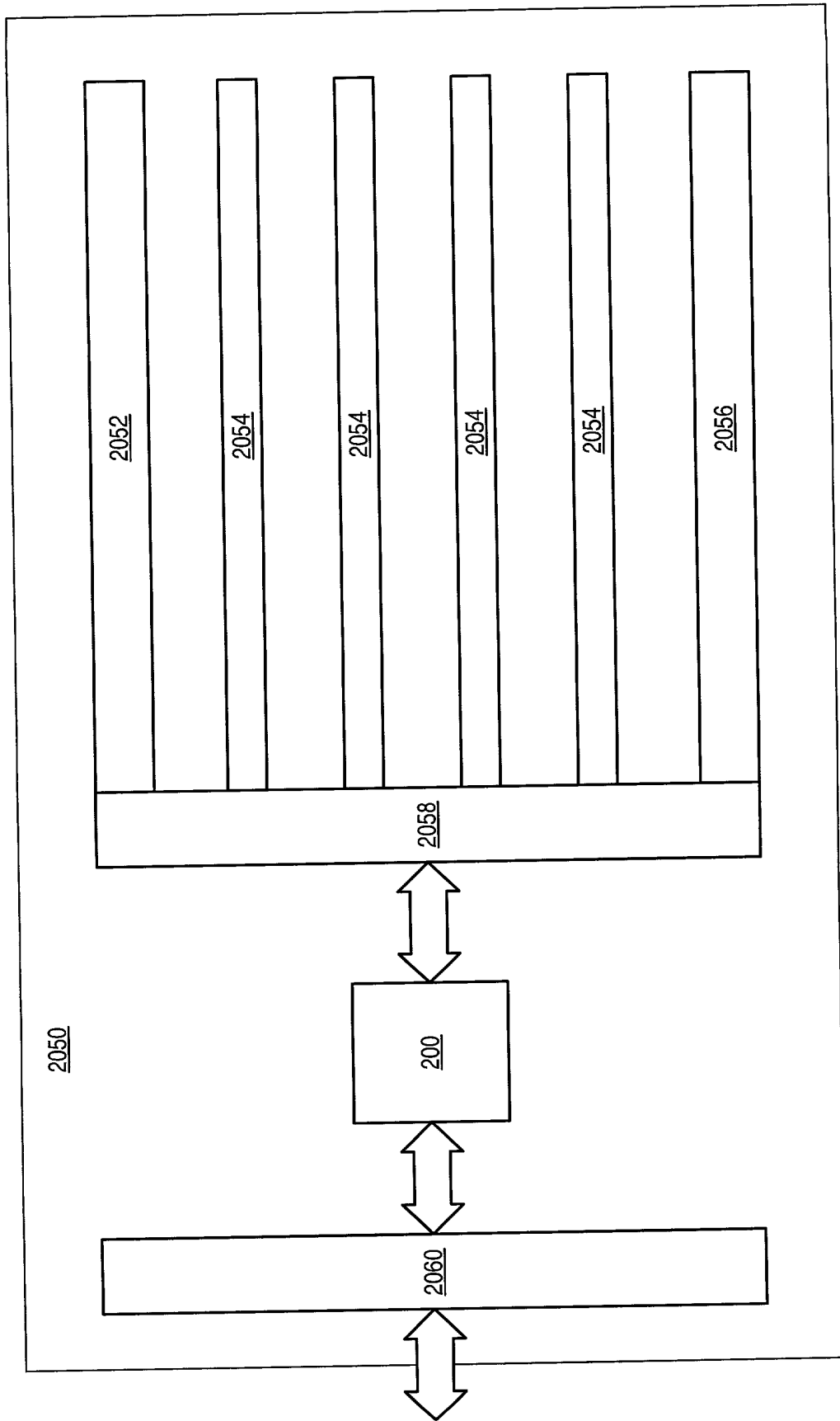


FIG. 46  
Solid State Storage Device

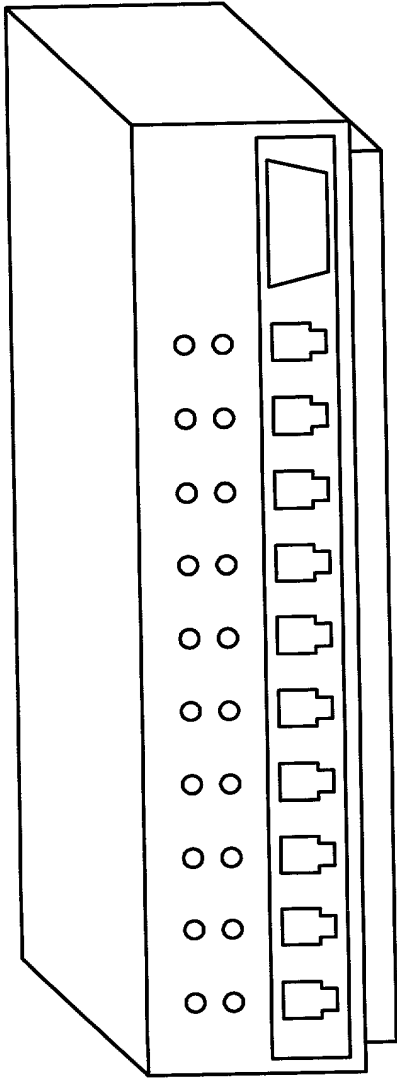


FIG. 47  
Network Hub

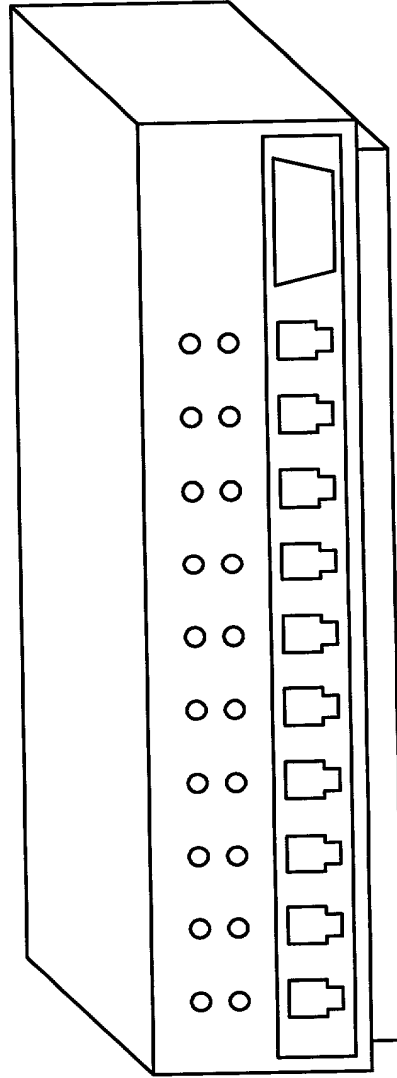


FIG. 48  
Network Switch

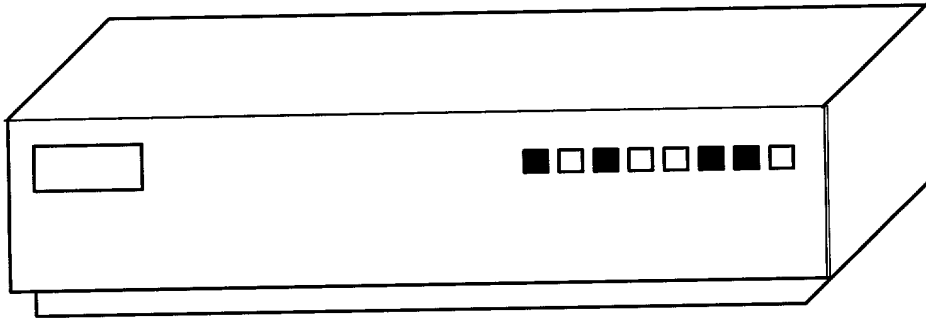


FIG. 49  
Network Bridge

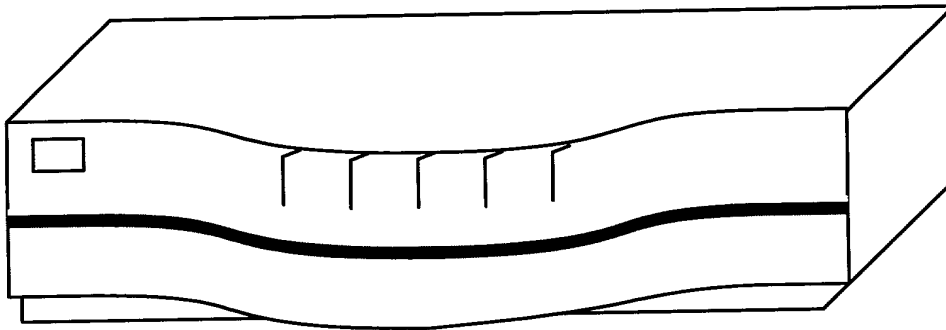


FIG. 50  
Network Router

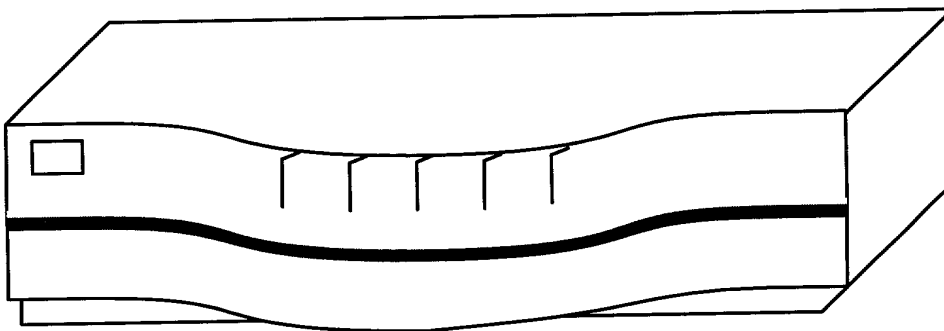


FIG. 51  
Network Brouter

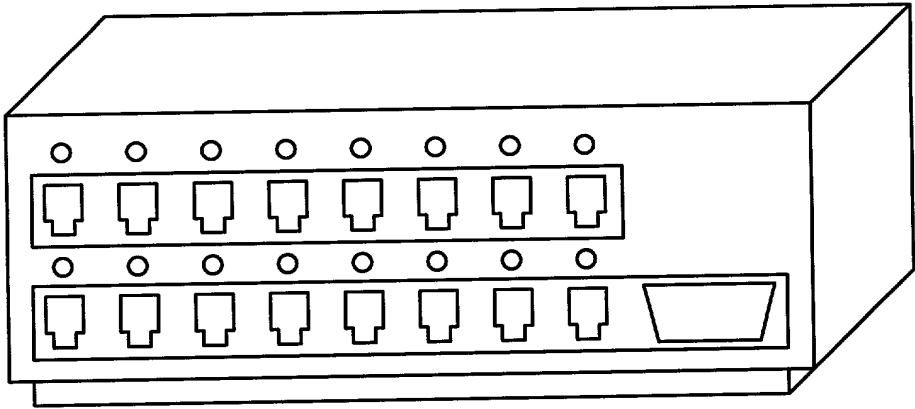


FIG. 52A  
Multiplexer

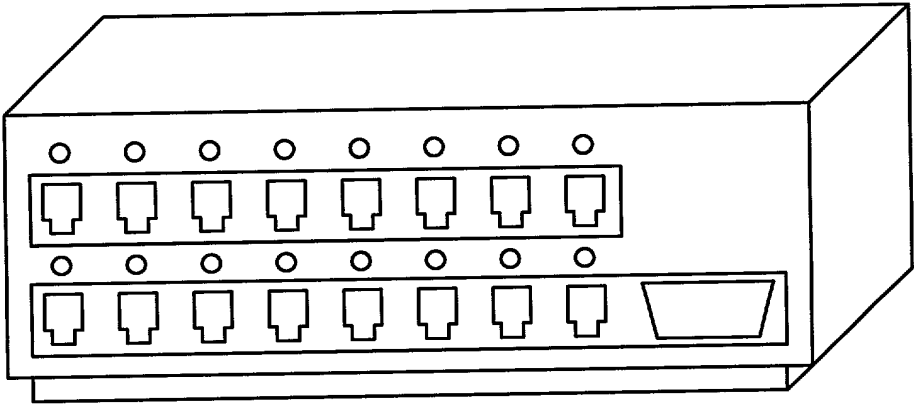


FIG. 52B  
Demultiplexer

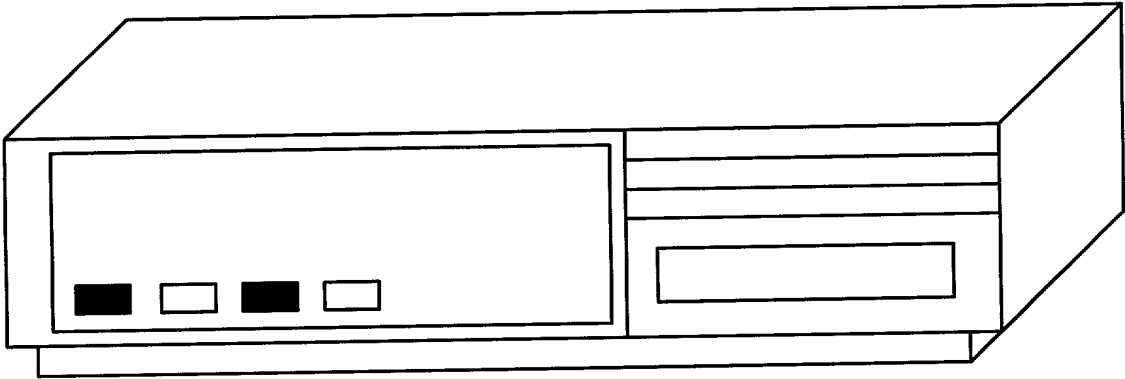


FIG. 53  
Terminal Server

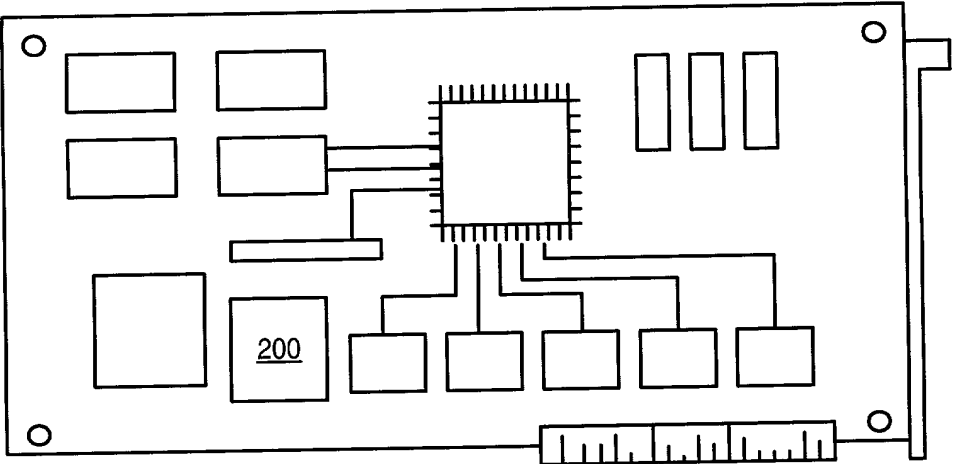


FIG. 54  
Network Interface Card

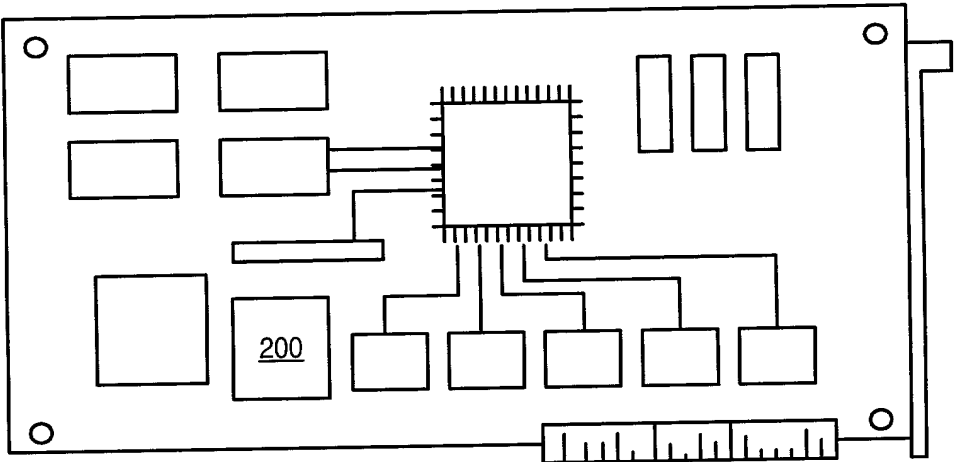


FIG. 55  
ISDN adapter

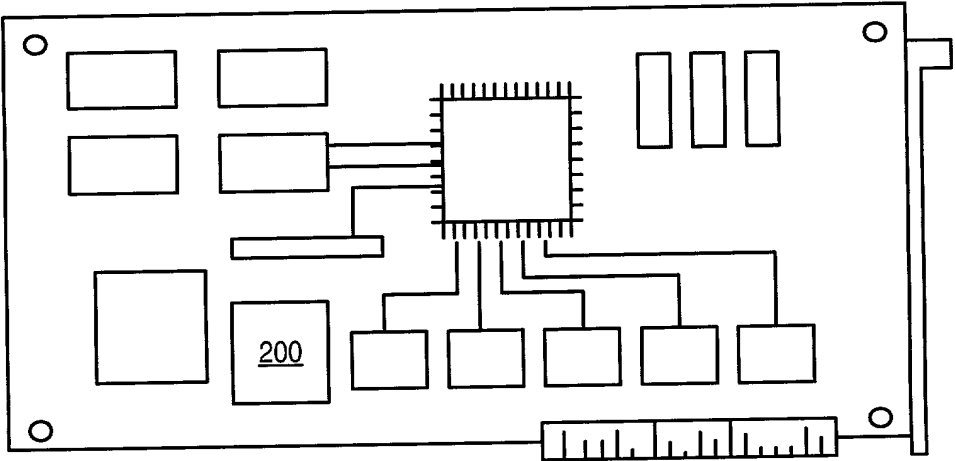


FIG. 56  
ATM adapter

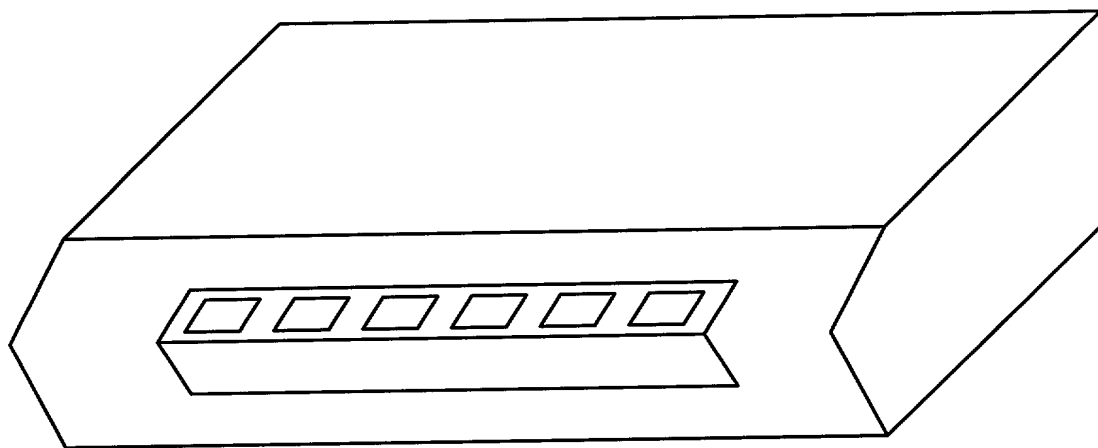


FIG. 57  
Modem

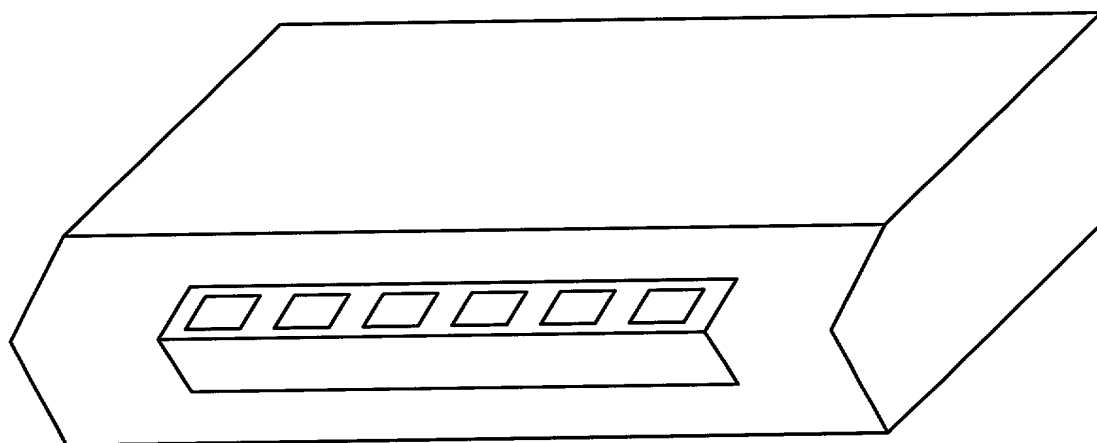


FIG. 58  
Cable modem

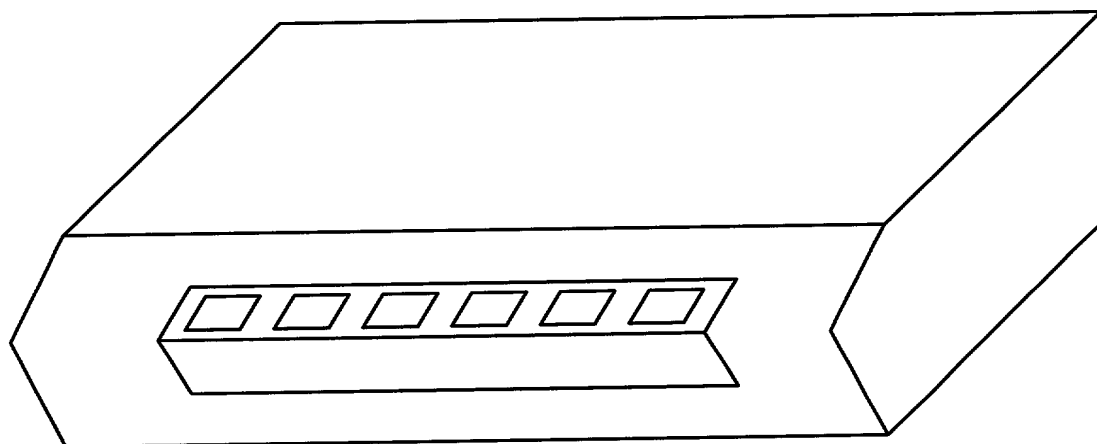


FIG. 59  
DSL adapter

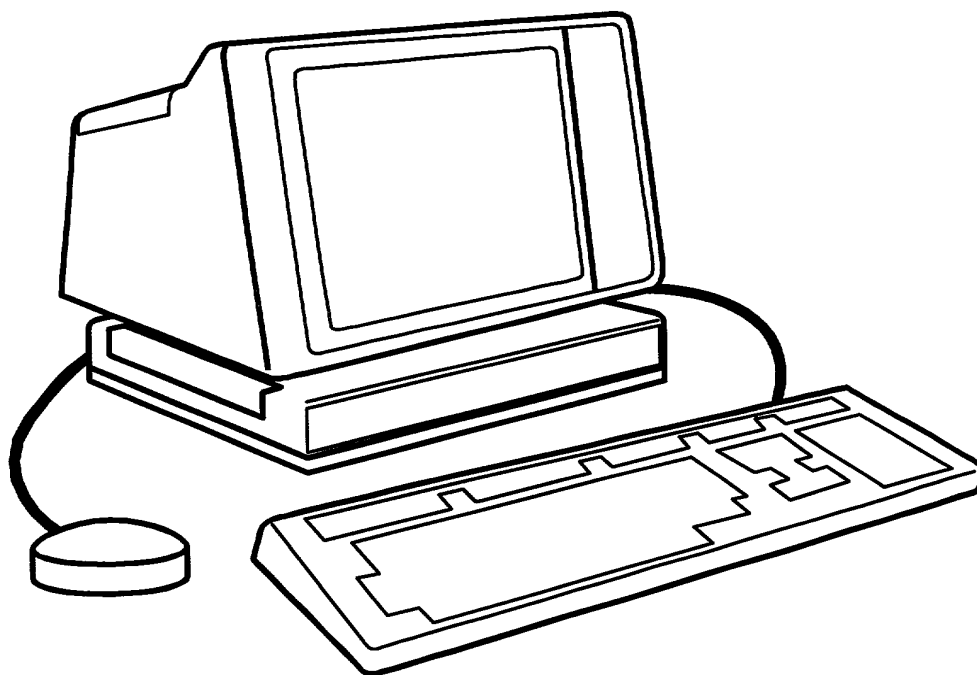


FIG. 60  
Network appliance

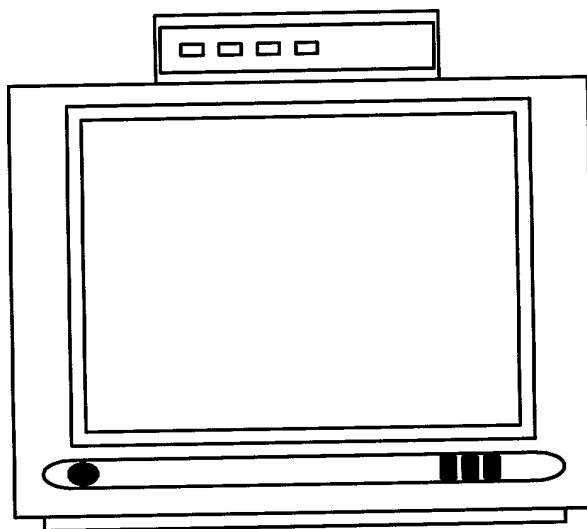


FIG. 61  
Television set with set top box

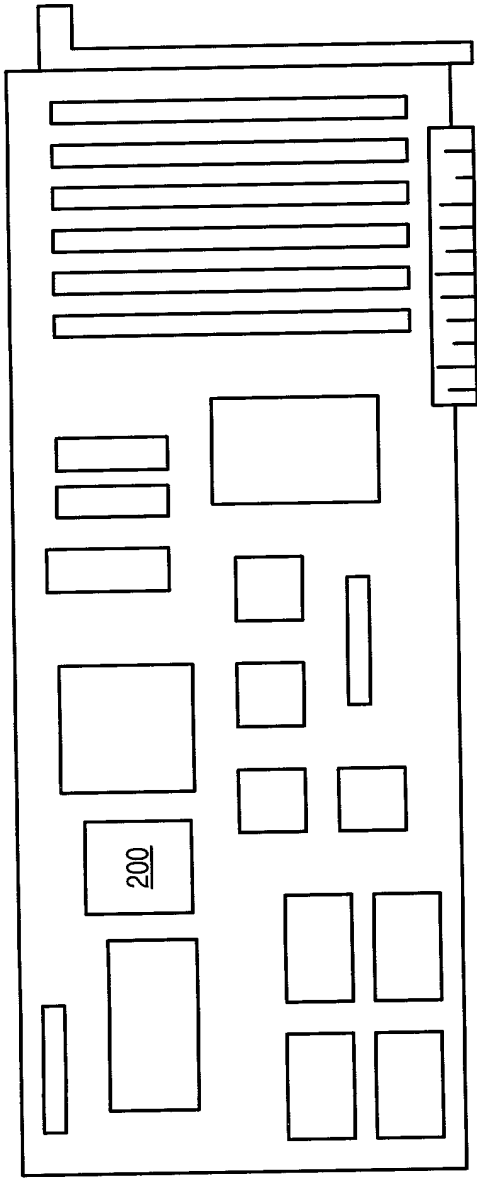


FIG. 62A  
Digital-to-Analog Card (DAC)

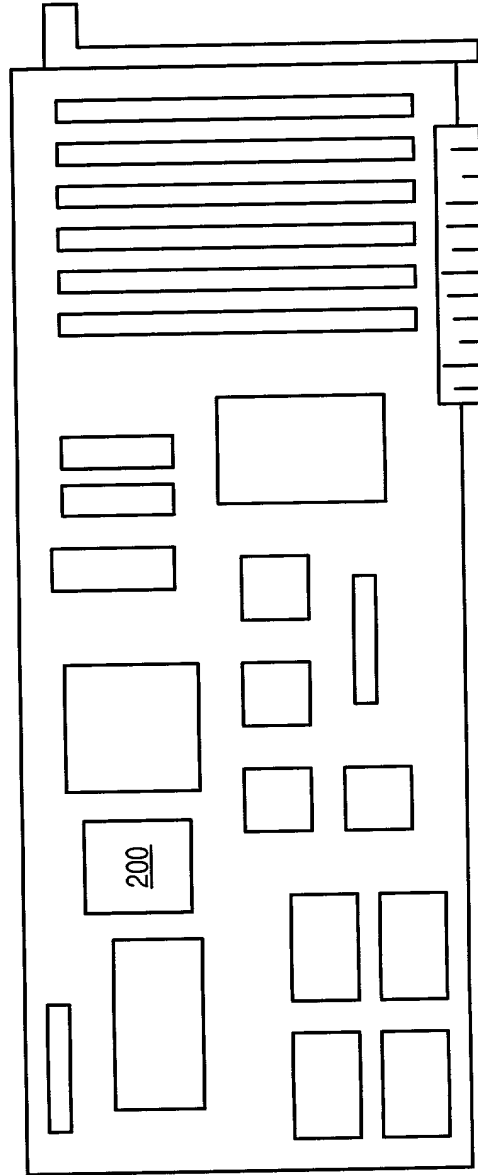


FIG. 62B  
Analog-to Digital Card (ADC)



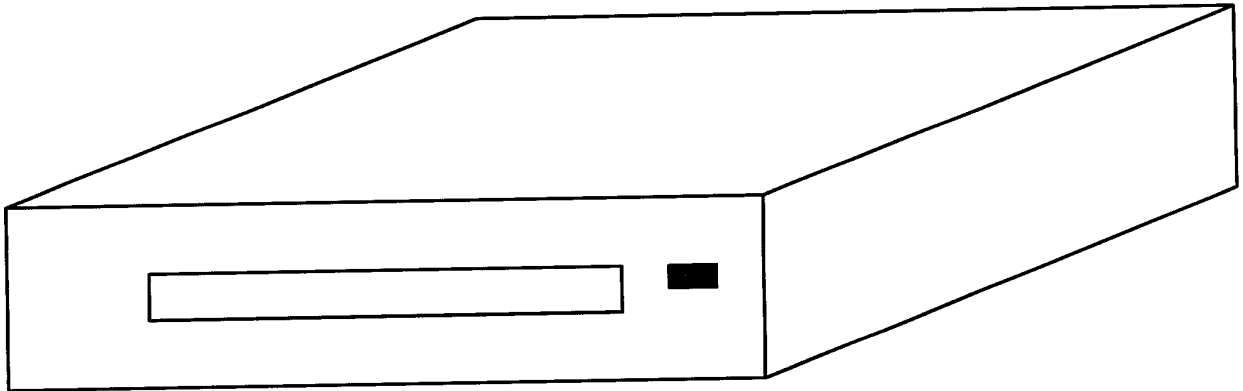


FIG. 63A  
Compact Disk (CD) Reader Device

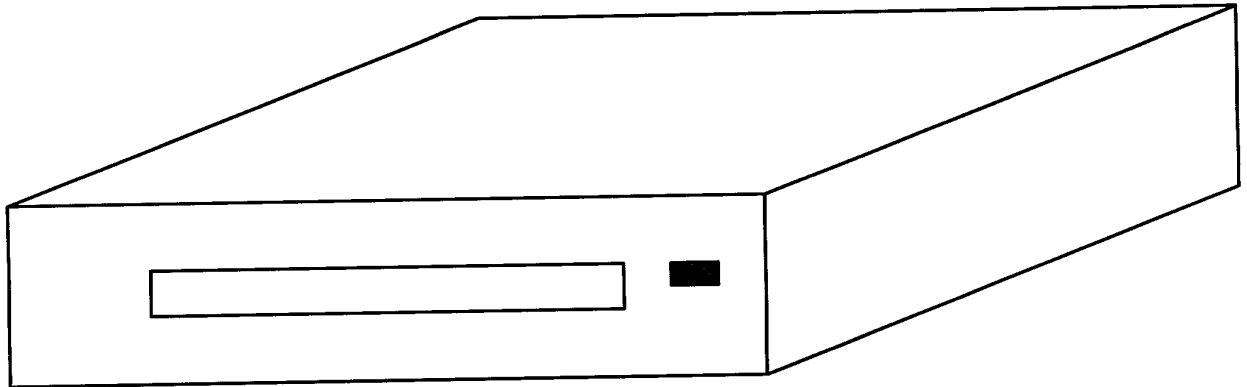


FIG. 63B  
CD-R Device

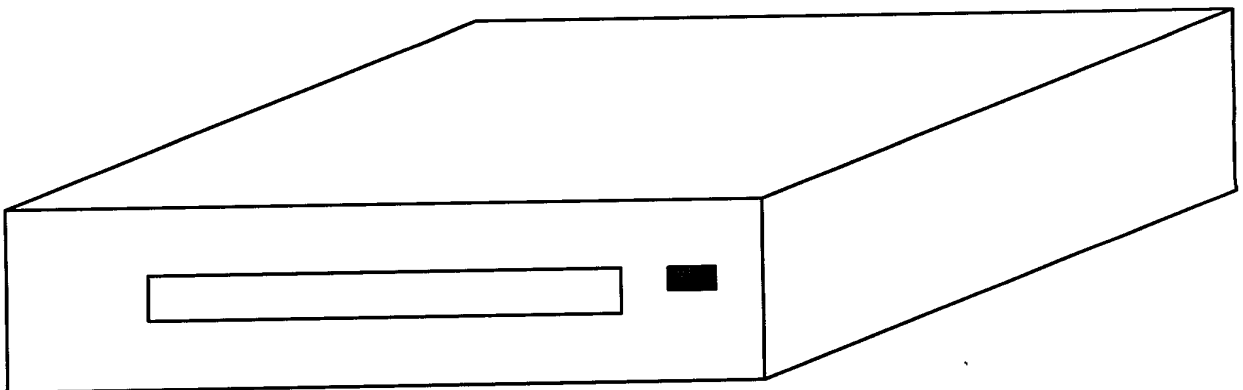


FIG. 63C  
CD-RW Device

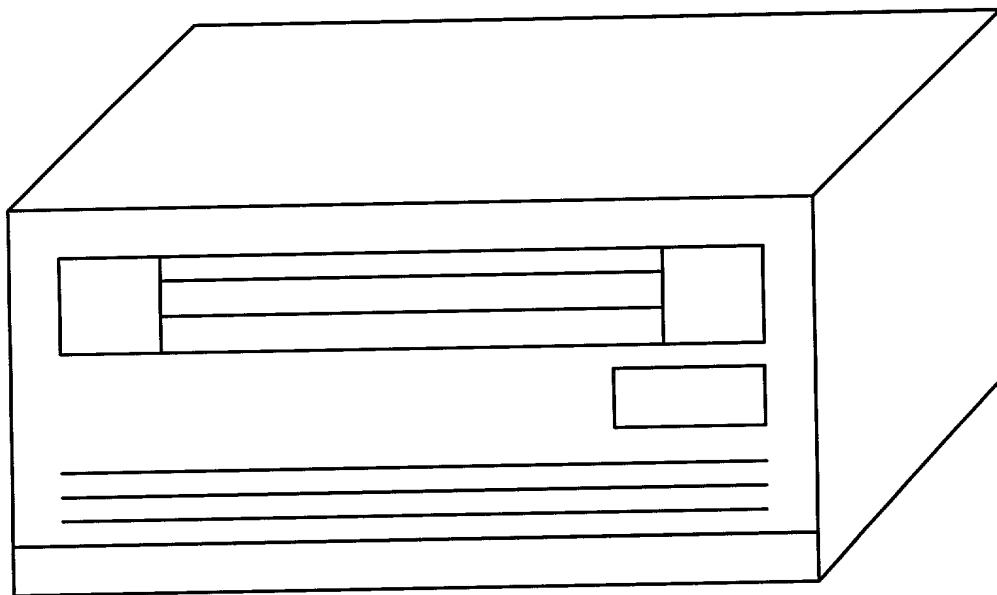


FIG. 64  
Optical Data Recording Device

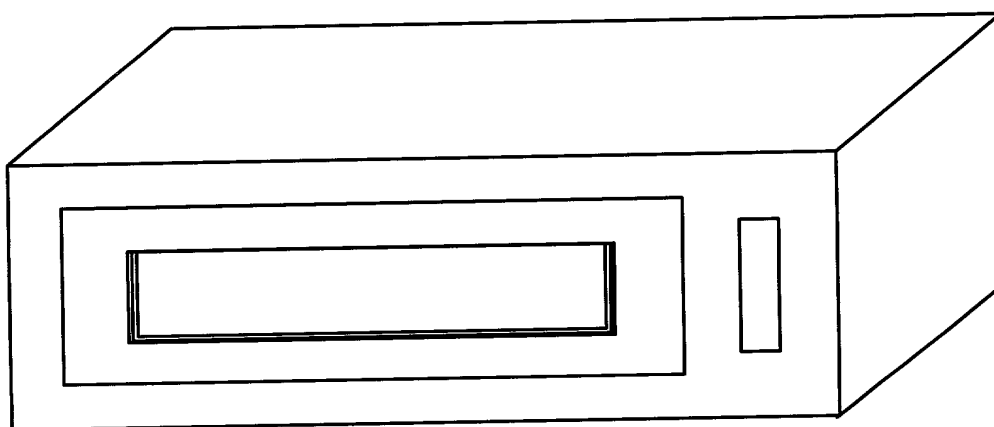


FIG. 65  
Digital Audio Recording Device

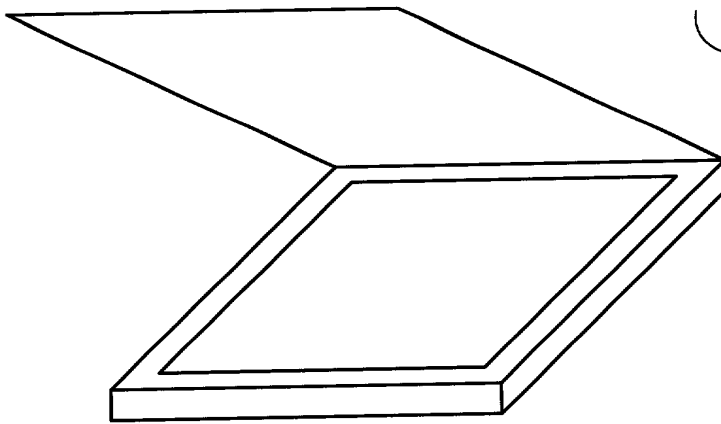


FIG. 66  
Scanner

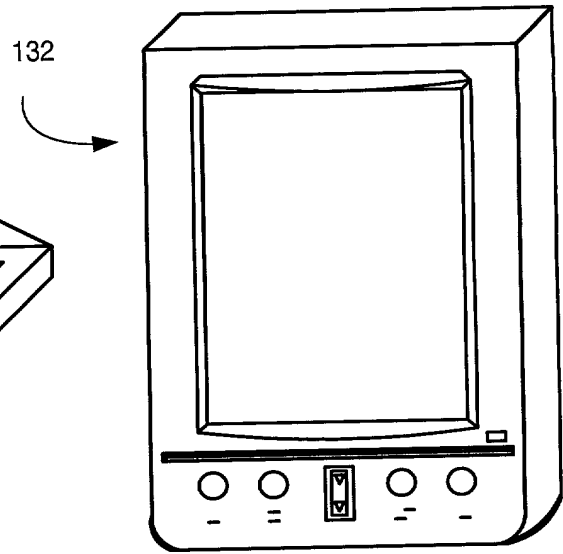


FIG. 67  
PDA

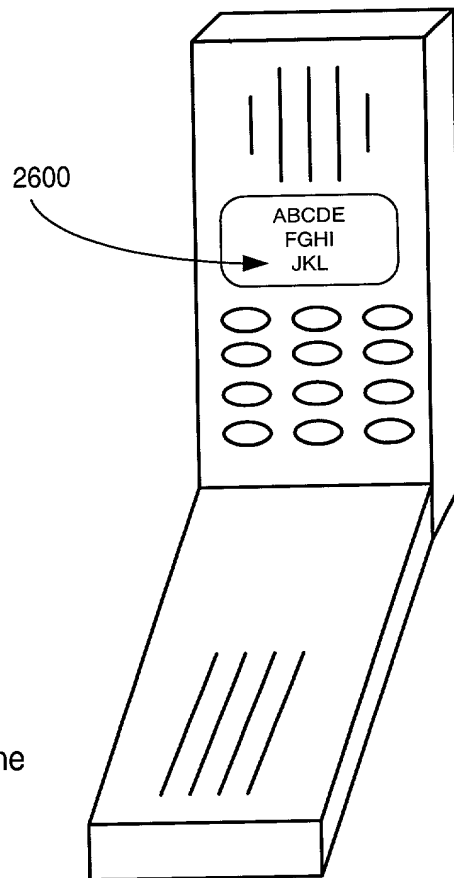


FIG. 68  
Cellular Telephone